GATE 2019

ANALOG CIRCUITS

ELECTRICAL ENGINEERING

ECG Publications

ECG Publications

A Unit of **ENGINEERS CAREER GROUP**

Head O ce: S.C.O-121-122-123, 2nd oor, Sector-34/A, Chandigarh-160022

Website: www.engineerscareergroup.in **Toll Free:** 1800-270-4242

E-Mail: ecgpublica ons@gmail.com | info@engineerscareergroup.in

GATE-2019: Analog Circuits| Detailed theory with GATE & ESE previous year papers and detailed solu ons.

First Edi on: 2016

Price of Book: *INR 630/-*

ECG PUBLICATIONS (A Unit of ENGINEERS CAREER GROUP) collected and proving data like: theory for di erent topics or previous year solu ons very carefully while publishing this book. If in any case inaccuracy or prin ng error may nd or occurred then **ECG PUBLICATIONS** (A Unit of ENGINEERS CAREER GROUP) owes no responsibility. The sugges ons for inaccuracies or prin ng error will always be welcome by us.

CONTENTS

CHAPTER - 1
DIODE CIRCUITS

1.1 INTRODUCTION

The simplest and most fundamental non-linear circuit element is a diode. Just like a resistor, the diode has two terminals but the diode has a non-linear i-v characteristics.

1.1.1 Diode Circuits

DC analysis and models. The ideal diode may be considered the most fundamental non-linear circuit element.

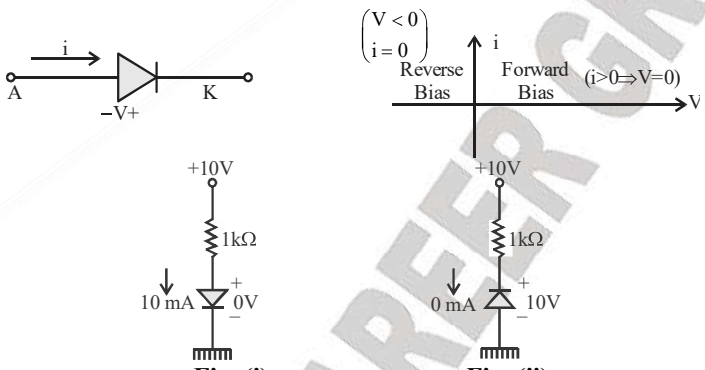


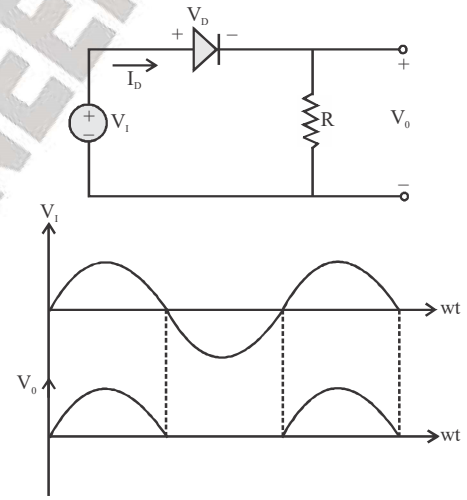
Fig. (i) Forward Current **Fig. (ii) Reverse Current**

In above fig(i) the diode is conducting. Thus its voltage drop will be zero and the current through it will be determined by the +10V supply and the 1 kΩ resistor as 10 mA.
In fig(ii) the diode is cut off and thus its current will be zero.

1.1.2 A Simple Applications

1.1.2.1 The Rectifier

The circuit consists of the series connection of a diode D and a resistor R.

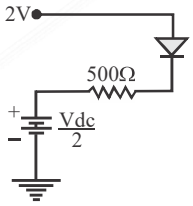


GATE QUESTIONS

1. An AC voltage source V = 10 sin (t) volts is applied to the following network. Assume that $R_1 = 3k\Omega$, $R_2 = 6k\Omega$ and $R_3 = 9k\Omega$ and that the diode is ideal.
Rms circuit I_{rms} (in mA) through the diode is _____

[GATE - 2017]

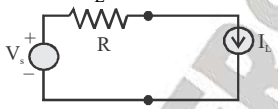
2. The silicon diode, shown in the figure, has a barrier potential of 0.7 V. There will be no forward current flow through the diode, if V_{dc}, in volt, is greater than



[GATE - 2017]

(a) 0.7 (b) 1.3
(c) 1.8 (d) 2.6

3. In the circuit shown below, V_s is a constant voltage source and I_L is a constant current load

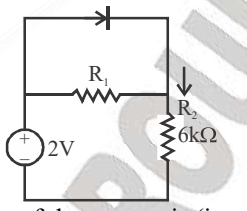


The value of I_L that maximizes the power absorbed by the constant current load is

[GATE - 2016]

(a) $\frac{V_s}{4R}$ (b) $\frac{V_s}{2R}$
(c) $\frac{V_s}{R}$ (d) ∞

4. Assume that the diode in the figure has V_{on} = 0.7 V, but is otherwise ideal.



The magnitude of the current i_2 (in mA) is equal to_____

[GATE - 2016]

5. The I-V characteristics of the zener diodes D1 and D2 are shown in figure 1. These diodes are used in the circuit given in figure II. If the supply voltage is varied from 0 to 100V, then breakdown occurs in

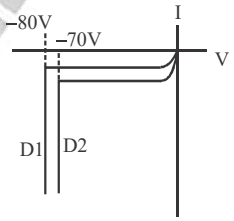


Figure I

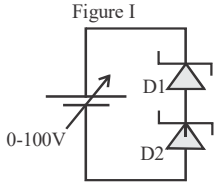


Figure II

[GATE - 2016]

(a) D1 only
(b) D2 only
(c) both D1 and D2
(d) none of D1 and D2

6. In the circuit shown, assume that the diodes D_1 and D_2 are ideal. The average value of voltage V_{ab} (in Volts), across terminals 'a' and 'b' is _____ .

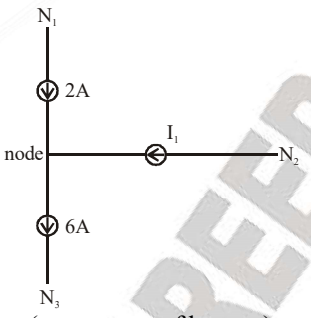
CHAPTER - 2
BJT BIASING AND SMALL SIGNAL ANALYSIS

2.1 BASIC OF NETWORK

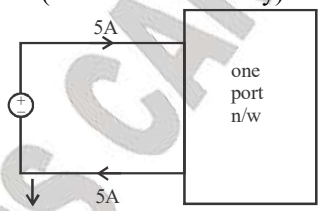
1. KCL
2. KVL
3. Nodal Analysis

Example.

$I_1 + 2 = 6$

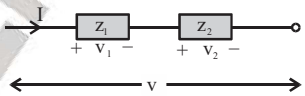


(current out of battery)



(current in battery)

1. Voltage Divider Rule

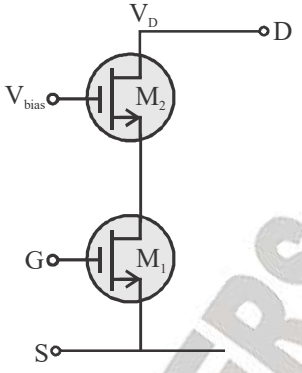


$$vl = \frac{v \times z_1}{z_1 + z_2}$$

Time Domain	Frequency Domain (s - domain)
R	Z=R
L	$Z_c(s)=Ls=j\omega L$
C	$Z_c(s)=\frac{1}{S_C}=\frac{1}{j\omega C}$

GATE QUESTIONS

1. Two identical nMOS transistors M_1 and M_2 are connected as shown below. The circuit is used as an amplifier with the input connected between G and S terminals and the output taken between D and S terminals, V_{bias} and V_D are so adjusted that both transistors
are in saturation. The transconductance of this combination is defined as g_m $g_m = \frac{\partial i_D}{\partial v_{GS}}$ while the output resistance is $r_0 = \frac{\partial v_{DS}}{\partial i_D}$, where i_D is the current flowing into the drain of M_2. Let g_{m1}, g_{m2} be the transcondcutances and r_{o1}, r_{o2} be the output resistance of transistors M_1 and M_2, respectively

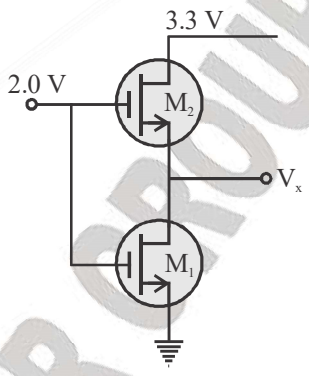


Which of the following statements about estimates for $g_m$and $r_0$is correct?

[GATE - 2018]

(a) $g_m \approx g_{m1} \cdot g_{m2} \cdot r_{02}$ and $r_0 \approx r_{01} + r_{02}$
(b) $g_m \approx g_{m1} + g_{m2}$ and $r_0 \approx r_{01} + r_{02}$
(c) $g_m \approx g_{m1}$ and $r_0 \approx r_{01} \cdot g_{m2} \cdot r_{02}$
(d) $g_m \approx g_{m1}$ and $r_0 \approx r_{02}$

2. In the circuit shown below, the (W/L) value for M_2 is twice that for M_1. The two nMOS transistors are otherwise identical. The threshold voltage V_T for both transistors is 1.0 V.
Note that V_{GS} for M_2 must be > 1.0 V



Current through the nMOS transistors can be modeled as

$$I_{DS} = \mu C_{ox}\left(\frac{W}{L}\right)\left((V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right) \text{ for } V_{DS} \le V_{GS} - V_T$$

$$I_{DS} = \mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)/2 \text{ for } V_{DS} \le V_{GS} - V_T$$

The voltage (in volts, accurate to two decimal places) at V_x is _____.

[GATE - 2018]

3. An npn biplar junction transistor (BJT) is operating in the active region. If the reverse bias across the base-collector junction is increased, then

[GATE - 2017]

(a) The effective base width increase and common-emitter current gain increases
(b) The effective base width increase and common-emitter current gain decreases
(c) The effective base width decrease and common-emitter current gain increases
(d) The effective base width decrease and common-emitter current gain decreases

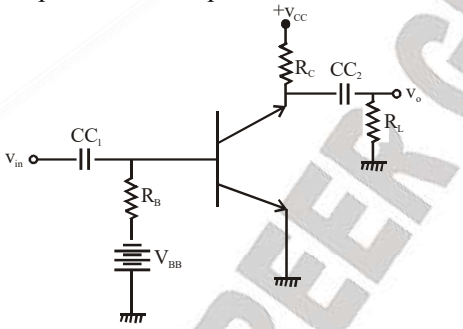
4. Consider the circuit shown in figure. Assume base to emitter voltage V_{BE} = 0.8V and common base current gain (α) of transistor is unity

CHAPTER - 3
FREQUENCY RESPONSE

3.1 CAPACITORS

There are three types of capacitors
1. Coupling Capacitor
2. Emitter Capacitor
3. Junction Capacitance/ Internal Capacitance

To determine the gain of amplifier with respect to itself frequency we need to do frequency analysis of amplifier in which response of the amplifier is studied over the range of frequency.



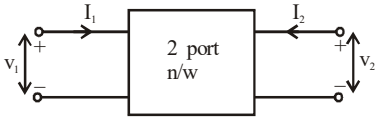
Slope of DC Load Line = $-\frac{1}{R_C}$

Slope of AC Load Line, m = $-\frac{1}{R_L'} = -\left(\frac{1}{R_C}+\frac{1}{R_L}\right)$

$\because \quad R_L' = \frac{1}{\left(\frac{1}{R_C}+\frac{1}{R_L}\right)}$

The slope of AC line is greater as compared to slope of DC line.

3.2 H-PARAMETER ANALYSIS OF BJT



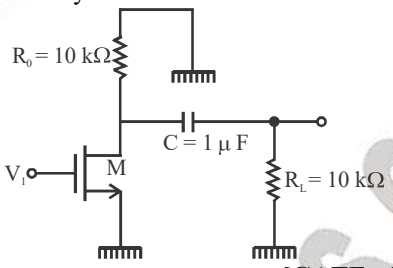
$V_1 = f(I, V_2)$
$I_2 = f(I, V_2)$
$V_1 = h_{11} I_1 + h_{12} V_2$
$I_2 = h_{21} I_1 + h_{22} V_2$

GATE QUESTIONS

1. For a superheterodyne receiver, the intermediate frequency is 15 MHz and the local oscillator frequency is 3.5 GHz. If the frequency of the received signal is greater than the local oscillator frequency, then the image frequency (in MHz) is_____

[GATE - 2016]

2. The ac schematic of an NMOS common-source stage is shown in the figure below, where part of the biasing circuits has been omitted for simplicity. For the n-channel MOSFET M, the transconductance gm = 1 mA/V, and body effect are to be neglected. The lower cut-off frequency in Hz of the circuit is approximately at



[GATE - 2013]

(a) 8 (b) 32
(c) 50 (d) 200

3. A bipolar transistor is operating in the active region with a collector current of 1 mA. Assuming that the β of the transistor is 100 and the thermal voltage (V_T) is 25 mV, the transconductance (gm) and the input resistance (rπ) of the transistor in the common emitter configuration, are

[GATE - 2004]

(a) g_m = 25mA/V and r_π = 15.625 kΩ
(b) g_m = 40mA/V and r_π = 4.0 kΩ
(c) g_m = 25mA/V and r_π = 2.5 kΩ
(d) g_m = 40mA/V and r_π = 2.25 kΩ

4. Three identical amplifiers with each one having a voltage gain of 50, input resistance of 1 kΩ and output resistance of 250 Ω, are cascaded. The open circuit voltage gain of the combined amplifier is

[GATE - 2004]

(a) 49 dB (b) 51 dB
(c) 98 dB (d) 102 Db

5. An npn BJT has g_m = 38 mA/V, $C_\mu = 10^{-14}$F, $C_\pi = 4 \times 10^{-13}$ F, and DC current gain β_0 = 90. For this transistor f_T and f_β are

[GATE - 2001]

(a) $f_T = 1.64 \times 10^8$ Hz and $f_\beta = 1.47 \times 10^{10}$ Hz
(b) $f_T = 1.47 \times 10^{10}$ Hz and $f_\beta = 1.47 \times 10^{10}$ Hz
(c) $f_T = 1.33 \times 10^{12}$ Hz and $f_\beta = 1.47 \times 10^{10}$ Hz
(d) $f_T = 1.47 \times 10^{10}$ Hz and $f_\beta = 1.33 \times 10^{12}$ Hz

6. An amplifier is assumed to have a single-pole high-frequency transfer function. The rise time of its output response to a step function input is 35 nsec. The upper-3 dB frequency (in MHz) for the amplifier to a sinusoidal input is approximately at

[GATE - 1999]

(a) 4.55 (b) 10
(c) 20 (d) 28.6

7. An npn transistor (with C = 0.3 pF0 has unity – gain cutoff frequency fT of 400 *** at a dc bias current Ic = 1 mA. The value of its Cμ (in pF) is approximately (VT = 26 m **) is

[GATE - 1999]

(a) 15 pF (b) 12 pF
(c) 17 pF (d) 10 pF

8. The fT of a BJT is related to its gm, Cπ and Cμ as follows

[GATE - 1996]

(a) $f_T = \dfrac{C_\pi + C_\mu}{g_m}$

(b) $f_T = \dfrac{2\pi(C_\pi + C_\mu)}{g_m}$

ESE OBJ QUESTIONS

1. The gain of a bipolar transistor drops at high frequencies. This is due to

[EC ESE-2018]

(a) Coupling and bypass capacitors
(b) Early effect
(c) Inter – electrode transistor capacitances
(d) The fact that reactance becomes high

2. The n-p-n transistor made of silicon has a DC base bias voltage 15 V and an input base resistor 150 KΩ. Then the value of the base current into the transistor is

[EC ESE-2017]

(a) 0.953μA (b) 9.53μA
(c) 95.3μA (d) 953μA

3. The capacitance of a full wave rectifier, with 60hz input signal, peak output voltage V_p = 10v, load resistance R = 10kΩ and input ripple voltage V_r = 0.2V, is

[EC ESE - 2016]

(a) 22.7 μF (b) 33.3 μF
(c) 41.7 μF (d) 83.4 μF

4. A full wave rectifier connected to the output terminals of the mains transformer produces and RMS voltage of 18V across the secondary. The no - load voltage across the secondary of the transformer is

[EC ESE - 2016]

(a) 1.62 V (b) 16.2 V
(c) 61.2 V (d) 6.12 V

5. A power supply uses bridge rectifier with capacitor input filter. If one of the diodes is defective, then
1. The dc load voltage will be lower than it expected value.
2. Ripple frequency will be lower than its expected value.
3. The surge current will increase manifold
Which of the above statements are correct?

[EC ESE - 2015]

(a) 1 and 2 only (b) 1 and 3 only
(c) 2 and 3 only (d) 1, 2 and 3

6. In an L-section filter , a bleeder resistance is connected across the load to

[EC ESE - 2015]

(a) Provide good regulation for all values of load
(b) Ensure lower PIV of the diodes
(c) Ensure lower values of capacitance in the filter
(d) Reduce ripple content

7. In a voltage regulator, zener diode is
1. connected in series with filter output
2. Forward biased
3. Connected in parallel with filter output
4. Reversed biased
Which of the above are correct

[EC ESE - 2015]

(a) 1 and 2 (b) 3 and 4
(c) 1 and 4 (d) 2 and 3

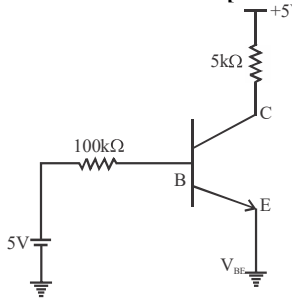
8. With the increase of reverse bias in a p-n diode, the reverse current

[EC ESE - 2013]

(a) Decreases
(b) Increases
(c) Remains constant
(d) May increase or decrease depending upon doping

9. The transistor as shown in the circuit is operating in:

[EC ESE - 2013]



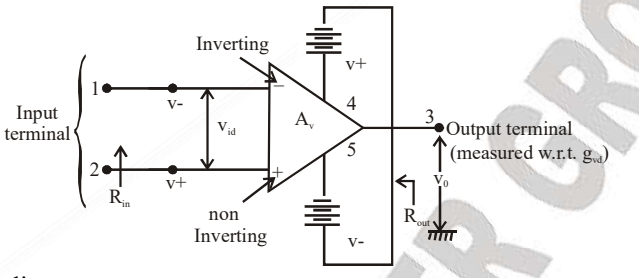
(a) Cut - off region
(b) Saturation region
(c) Active region
(d) Either in active or saturation region

CHAPTER - 4
OPERATIONAL AMPILIFIER AND APPLICATIONS

4.1 INTRODUCTION

Operational amplifier is a d.c. coupled high gain voltage amplifier.

Operational amplifier is available in IC form and it can be obtained in 7 pin ICs or more than 14 pin IC's and many more.

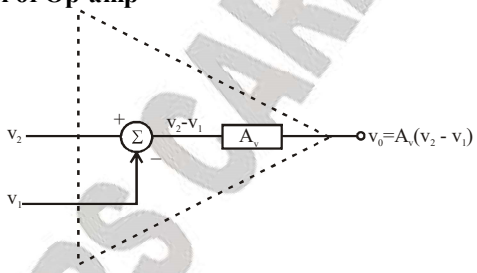


v^+ and v^- are d.c. supplies

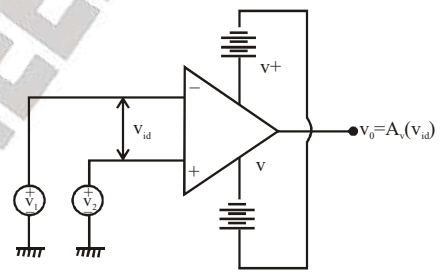
v^+ and v^- are the two dc power supplies which are necessary for its working.

$v_{id} = v_+ - v_-$

4.1.1 Mathematical Model of Op-amp



Op-amp is design to sense the difference between voltage signal to applied between its two input signal.



v_1 and v_2 are the voltage applied w.r.t ground.

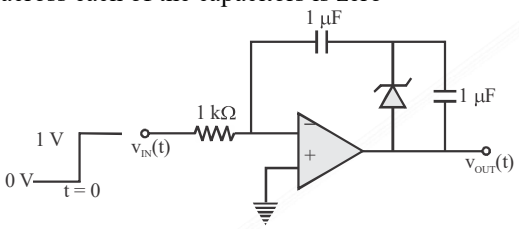
If $v_1 = v_2 = v$ $\therefore$ $v_o = Av\ [\ v - v\ ] = 0$.

If we provide same input at both end then the output will be zero ideally.

Hence in ideal op-amp common voltage should be zero.

GATE QUESTIONS

1. In the circuit shown below, the op-amp is ideal and Zener voltage of the diode is 2.5 volts. At the input, unit step voltage is applied i.e.$v_{IN}(t) = u(t)$ volts. Also at t = 0, the voltage across each of the capacitors is zero

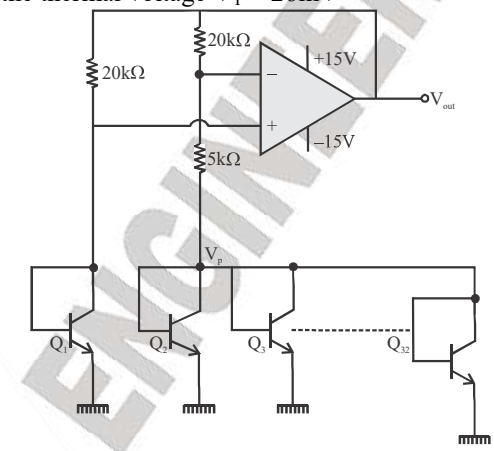


The time t, in milliseconds, at which the output voltage v_{OUT} crosses −10 V is

[GATE - 2018]

(a) 2.5 (b) 5
(c) 7.5 (d) 10

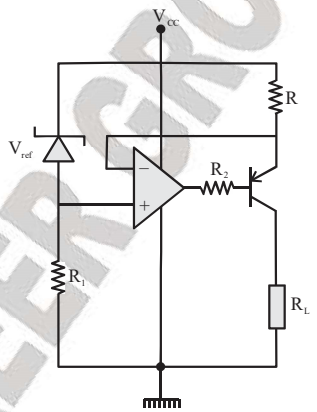
2. In the voltage reference circuit shown in the figure, the op-amp is ideal and transistors Q_1, Q_2 ……, Q_{32} are identical in all respects and have infinitely large values of common-emitter current gain (β). The collector current (I_c) of the transistors is related to their base emitter voltage (V_{BE}) by the relation $I_C = I_S \exp(V_{BE}/V_T)$; where I_s is the saturation current. Assume that the voltage V_p shown in the figure is 0.7V nad the thermal voltage V_T = 26mV



The output voltage Vout (in volts) is _____

[GATE - 2017]

3. Consider the constant current source shown in the figure below. Let β represent the current gain of the transistor



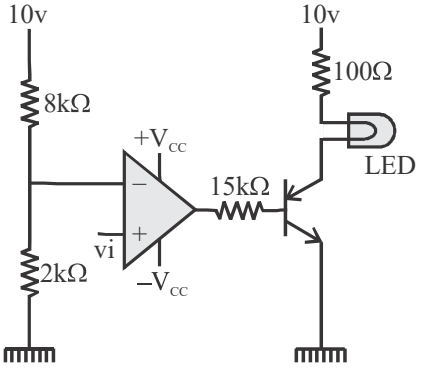
The load current I_0 through RL is

[GATE - 2017]

(a) $I_0 = \left(\frac{\beta+1}{\beta}\right)\frac{V_{ref}}{R}$ (b) $I_0 = \left(\frac{\beta}{\beta+1}\right)\frac{V_{ref}}{R}$

(c) $I_0 = \left(\frac{\beta+1}{\beta}\right)\frac{V_{ref}}{2R}$ (d) $I_0 = \left(\frac{\beta}{\beta+1}\right)\frac{V_{ref}}{2R}$

4. The following signal V_i of peak voltage 8V is applied to the non-inverting terminal of an ideal Opamp. The transistor has V_{BE} = 0.7V, β = 100; V_{LED} = 1.5V, V_{CC} = 10V and $-V_{CC}$ = −10V.



CHAPTER - 5
FEEDBACK AMPLIFIER AND OSCILLATOR

5.1 FEEDBACK ARE OF TWO TYPES

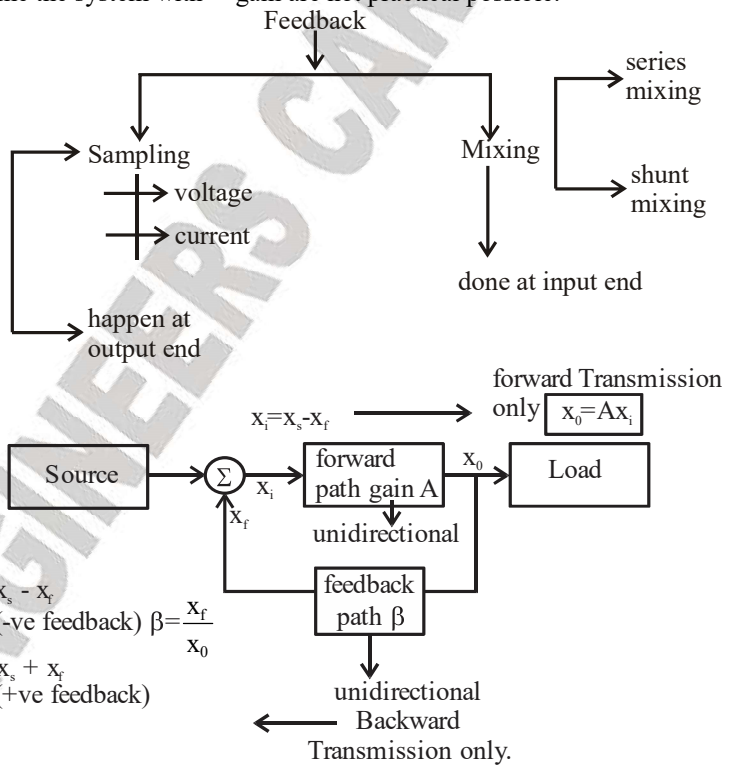
1. Regenerative feedback [+ve (oscillators) feedback]
2. Degenerative feedback [–ve (amplifier) feedback]

In amplifier design negative feedback is applied to effect one or more of the following property
Feedback in practical case is never 100%.
Feedback decide the fraction of output which is given back to the input.

5.1.1 General structure of the feedback

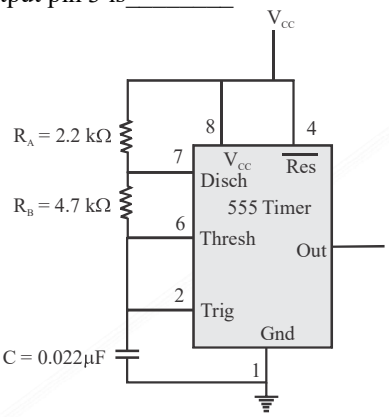
1. Gain $= \frac{\text{output}}{\text{input}} \Rightarrow$ finite [for all practical stable system]
2. Gain = finite $\rightarrow$ mean output following input
3. Gain $\Rightarrow \infty \Rightarrow \frac{\text{finite}}{\text{zero}} \rightarrow \frac{\text{output}}{\text{input}} \Rightarrow$ unstable system

If gain is finite then output is finite for zero input. If this arrangement is intended arrangement then the system arrangement is stable. If the gain f the system become finite by chance then the system is unstable became the system with ∞ gain are not practical possible.



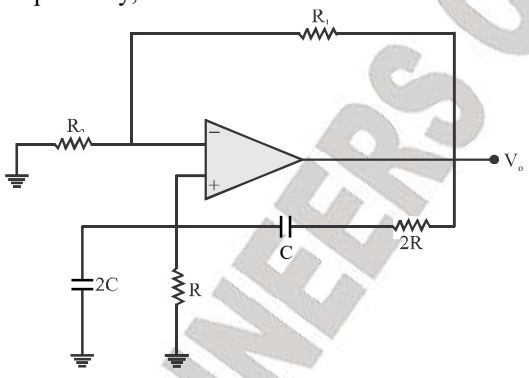
GATE QUESTIONS

1. In the table multivibrator circuit shown in the figure, the frequency of oscillation (in kHz) at the output pin 3 is_____



[GATE - 2016]

2. The circuit shown in the figure has an ideal opamp. The oscillation frequency and the condition to sustain the oscillations, respectively, are



[GATE - 2015]

(a) $\frac{1}{CR}$ and $R_1 = R_2$

(b) $\frac{1}{CR}$ and $R_1 = 4R_2$

(c) $\frac{1}{2CR}$ and $R_1 = R_2$

(d) $\frac{1}{2CR}$ and $R_1 = 4R_2$

3. The desirable characteristics of a transconductance amplifier are

[GATE - 2014]

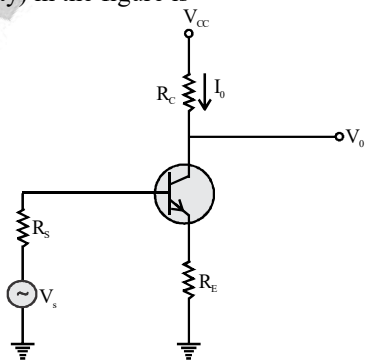
(a)High input resistance and high output resistance

(b)High input resistance and low output resistance

(c)Low input resistance and high output resistance

(d)Low input resistance and low output resistance

4. The feedback topology in the amplifier circuit (the base bias circuit is not shown for simplicity) in the figure is



[GATE - 2014]

(a) Voltage shunt feedback

(b) Current series feedback

(c) Current shunt feedback

(d) Voltage series feedback

5. In the ac equivalent circuit shown in the figure, if i_{in} is the input current and R_F is very large, the type of feedback is

ESE OBJ QUESTIONS

1. An amplifier, without feedback, has a gain A. The distortion at full output is 10%. The distortion is reduced to 2% with negative feedback (feedback factor $\beta = 0.03$). The values of A and A′(i.e, the gain with feedback) are, respectively, nearly

[EC ESE - 2018]

(a) 133.3 and 18.5 (b) 133.3 and 26.7
(c) 201.3 and 26.7 (d) 201.3 and 18.5

2. In a sinusoidal oscillator, sustained oscillator will be produced only if the loop gain (at the oscillation frequency) is

[EC ESE - 2016]

(a) Less than unity but not zero
(b) Zero
(c) Unity
(d) Greater than unity

3. Consider the following statements regarding Wien Bridge oscillator:
1. It has a larger banwidth than the phase shift oscillator
2. It has a smaller bandwidth than the phase shift oscillator
3. It has 2 capacitor while the phase shift oscillator has 3 capacitors.
4. It has 3 capacitors while the phase shift oscillator has 2 capacitors.
Which of the above statements are correct ?

[EC ESE - 2016]

(a) 1 and 3 only (b) 2 and 4 only
(c) 1 and 4 only (d) 2 and 3 only

4. If the quality factor of a single-tuned amplifier is doubled, the bandwidth will

[EC ESE - 2016]

(a) Remain the same
(b) Become ball
(c) Become double
(d) Become four times

5. Consider the following statements related to oscillator circuits.
1. The tank circuit of a Hartley oscillator is made up of a tapped capacitor and a common inductor.
2. The than circuit of a Colpitts oscillator is made up of a tapped capacitor and a common oscillator.
3. The wien bridge oscillator is essentially a two -stage amplifier with an RC bridge in the first stage and the second stage serving as an inverter.
4. Crystal oscillators are fixed frequency oscillators with a high Q - factor.
Which of the above statements are correct?

[EC ESE - 2016]

(a) 1, 2 and 3 only (b) 2, 3 and 4 only
(c) 1, 2 and 4 only (d) 1, 3 and 4 only

6. A negative feedback of $\beta = 2.5 \times 10^{-3}$ is applied to an amplifier of open-loop gain 1000. What is the change in overall gain of the feedback amplifier, if the gain of the internal amplifier is reduced by 20%?

[EE ESE - 2016]

(a) 295.7 (b) 286.7
(c) 275.7 (d) 266.7

7. In order to generate a square wave form a sinusoidal input signal ,one can use

[EE ESE - 2015]

1. Schmitt trigger circuit
2. Clippers and amplifiers
3. Monostable multivibrator
Which of the above statements are correct?
(a) 1, 2 and 3
(b) 1 and 2 only
(c) 1 and 3 only
(d) 2 and 3 only

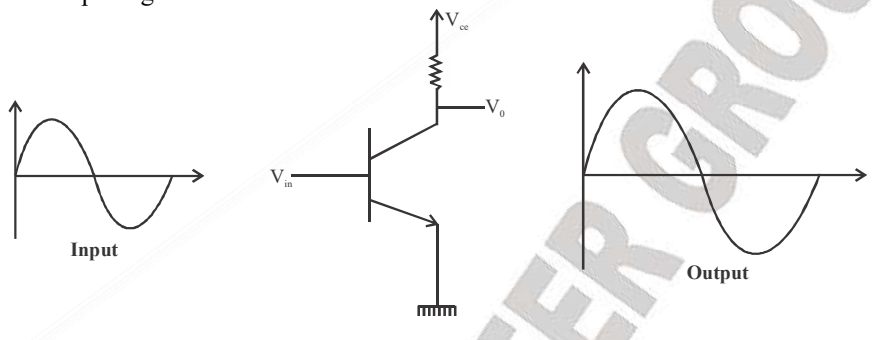
8. In a voltage-series feedback amplifier with open loop gain A_v and the feedback factor β, the input resistance becomes

[EE ESE - 2015]

CHAPTER - 6
POWER AMPLIFIERS

6.1 POWER AMPLIFIER/LARGE SIGNAL AMLIFIER

1. It is the last stage in multistage amplifier.
2. It is defined as ability of amplifier to convert available output dc power into ac power with the application of input signal.



6.2 HARMONIC DISTORTION

1. In a power amplifier, signal amplitudes is very large. Hence signal is operated in linear & non-linear portion of input characteristics. So we get harmonics in output and harmonic distortion is present at output.
2. It is a non-linear distortion.
3. Fourier series expansion of collator current of power transistor is:

$i_c = I_c + B_0 + B_1\cos\omega t + B_2\cos 2\omega t + \ldots\ldots$

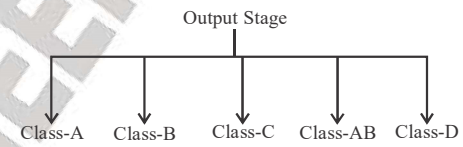
where $I_c + B_0$ is DC

$B_1\cos\omega t$ is fundamental

$B_2\cos 2\omega t$ is harmonics

6.3 CLASSIFICATION OF OUTPUT STAGE

Output stages are classified according to the collector current wave form that result when an input is applied



Second harmonic distortion, $D_2 = \left|\frac{B_2}{B_1}\right|$

Third harmonic distortion, $D_3 = \left|\frac{B_3}{B_1}\right|$

AC power output due to fundamental component

$$P_{ac} = I_{rms}^2 R_0 = \left(\frac{B_1^2}{2}\right) R_0 \Rightarrow P_1$$

GATE QUESTIONS

1. Which one of the following statements is correct about an ac-coupled common-emitter amplifier operating in the mid band region?

[GATE - 2016]

(a) The device parasitic capacitances behave like open circuits, whereas coupling and bypass capacitances behave like short circuits.
(b) The device parasitic capacitances coupling capacitances and bypass capacitances behave like open circuits.
(c) The device parasitic capacitances, coupling capacitances and bypass capacitances behave like short circuits.
(d) The device parasitic capacitances behave like short circuits, whereas coupling and bypass capacitances behave like open circuits.

2. Crossover distortion behavior is characteristic of

[GATE - 1999]

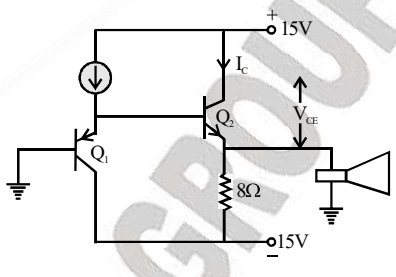
(a) Class A output stage
(b) Class B output stage
(c) Class AB output stage
(d) Common-base output stage

3. A power Amplifier delivers 50 W output at 50% efficiency. The ambient temperature is 25ºC. If the maximum allowable junction temperature is 150ºC, then the maximum thermal resistance θg_c that can be tolerated is _____ .

[GATE - 1995]

4. The circuit shown in the figure supplies power to on 8Ω speaker, LS. The values of I_C and V_{CE} for this circuit will be I_C = _____ and V_{CE} = _____ .

[GATE - 1995]



5. A class-A transformer coupled, transistor power Amplifier is required to deliver a power output of 10 watts. The maximum power Rating of the transistor should not be less than

[GATE - 1994]

(a) 5W (b) 10W
(c) 20W (d) 40W

6. In a transistor push-pull Amplifier

[GATE - 1993]

(a) There is no d.c. present in the output
(b) There is no distortion in the output
(c) There is no even harmonics in the output
(d) There is no add harmonics in the output

7. In case of class A amplifiers the ratio (efficiency of transformer coupled amplifier)/(efficiency of a transformer less amplifier) is

[GATE - 1987]

(a) 2.9 (b) 1.36
(c) 1.0 (d) 0.5

ESE OBJ QUESTIONS

1. The Class-B- pull amplifier is an efficient two-transistor circuit, in which the two transistors operate in the following way:

[EE ESE - 2016]

(a) Both transistors operate in the active region throughout the negative ac cycle

(b) Both transistors operate in the active region for more than half – cycle but less than a whole cycle

(c) One transistor conducts during the positive half-cycle and the other during the negative half-cycle

(d) Full supply voltage appears across each of the transistors

2. Which of the following is the principal factor that contributes to the doubling of the conversion efficiency in a transformer coupled amplifier?

[EE ESE - 2015]

(a) Reducing the power dissipated in the transistor

(b) Eliminating the power dissipation in the transformer

(c) Elimination of dc power dissipated in the load

(d) Impedance matching of the transformer

3. A power amplifier operated from 12v battery gives an output of 2W. The maximum collector current in the circuit is

[EC ESE - 2015

(a) 166.7 μA (b) 166.7mA

(c) 166.7 mA (d) 16.67 mA

4. For a transformer, the load connected to the secondary has an impedance of 8Ω. Its reflected impedance on primary is observed to be 648Ω. The turns ratio of this transformer is

[EE ESE - 2014]

(a) 6 : 1 (b) 10 : 1

(c) 9 : 1 (d) 8 : 1

5. A power amplifier with a gain of $100\angle 0°$ has an output of 12v at 1.5 kHz along with a second harmonic content of 25 percent. A negative feedback is to be provided to reduce the harmonic content of the output to 2.5 percent. What should be the gain of the feedback path and the level of signal input to the overall system, respectively ?

[EE ESE - 2014]

(a) 0.9 and 0.12 V (b) 0.9 and 12 V

(c) 0.09 and 1.2 V (d) 9 and 0.12V

6. An output signal of a power amplifier has amplitudes of 2.5 V fundamental, 0.25 V, second harmonic and 0.1 V third harmonic. The total percentage harmonic distortion of the signal is

[EC ESE - 2012]

(a) 12.8% (b) 10.8%

(c) 6.4% (d) 1.4%

7. The second-harmonic component in the output of a transistor amplifier, without feedback, is B_2. The second harmonic component, with negative feedback B_2' is equal to (where A = Amplifier gain and β = feedback factor).

[EC ESE - 2012]

(a) $\frac{B_2}{1+A\beta}$ (b) $B_2(1 + A\beta)$

(c) $\frac{B_2}{\beta}$ (d) $\frac{B_2}{A\beta}$

8. Statement (I) : Much of the distortion introduced in large signal amplifiers is eliminated by push –pull circuit

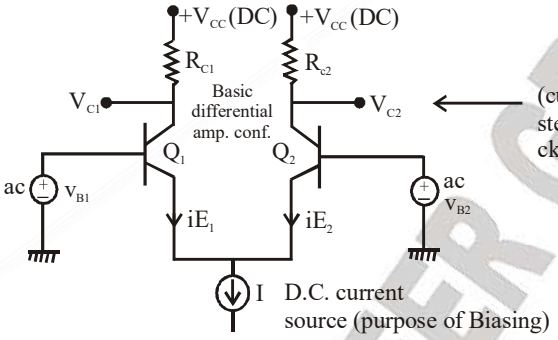
Statement (II) : The signals applied to the two transistors applied to the two transistors in push -pull mode are 180° out of phase

[EE ESE - 2012]

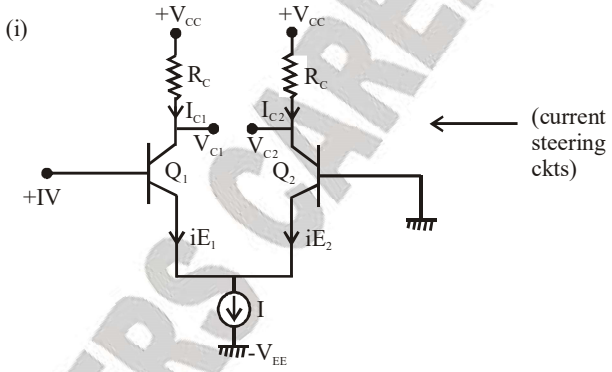
CHAPTER - 7
DIFFERENTIAL AMPLIFIERS

7.1 DIFFERENTIAL AMPLIFIER (BJT PAIR)

It is also known as emitter coupled differential amplifier. It consist of 2 matched transistor Q_1 and Q_2, whose emitters are joined together.



(i)

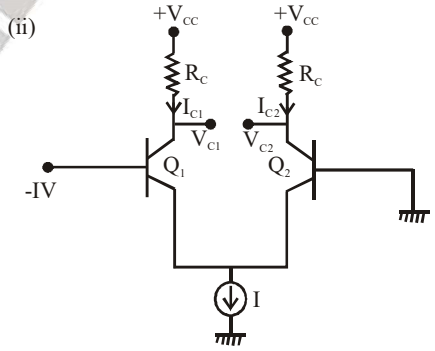


$$\frac{v_{cc} - v_{c1}}{R_c} = I_{c_1}$$

$v_{cc} - I_{c1}R_c = v_{c1}$

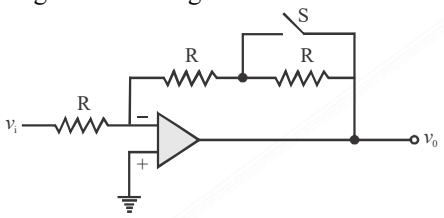
$v_{cc} - I_{c2}R_c = v_{c2}$

(ii)



ESE OBJ QUESTIONS

1. The magnitude of the gain $\frac{V_0}{V_i}$ in the inverting op-amp circuit shown in the figure is x with switch S open. When switch S is closed, the magnitude of the gain will be



[EE ESE - 2018]

(a) x (b) $\frac{x}{2}$

(c) 2x (d) $\frac{2}{x}$

2. An op-amp is used in a notch filter. The notch frequency is 2 kHz, lower cut-off frequency is 1.8 kHz and upper cut-off frequency is 2.2 kHz. Then Q of the notch filter is

[EE ESE - 2018]

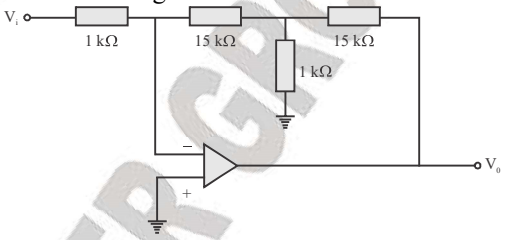
(a) 3.5 (b) 4.0
(c) 4.5 (d) 5.0

3. In op-amp based inverting amplifier with a gain of 100 and feedback resistance of 47kΩ, the op – amp input offset voltage is 6 mV and input bias current is 500 nA. The output offset voltage due to an input offset voltage and an input bias current, are

[EE ESE - 2018]

(a) 300 mV and 23.5 mV
(b) 606 mV and 47.0 mV
(c) 300 mV and 47.0 mV
(d) 606 mV and 23.5 mV

4. What is the gain of the amplifier circuit as shown in the figure?



[EE ESE - 2018]

(a) 255 (b) 31
(c) –31 (d) –255

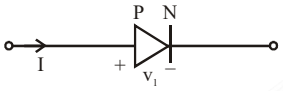
5. Statement (I) :
In ideal case, the inverting and non-inverting input terminals of an operational amplifier are almost at the same potential.
Statement (II) :
It is common practice to connect the inverting and non – inverting terminals to the same point.
Codes:

[EE ESE - 2018]

(a) Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I)
(b) Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I)
(c) Statement (I) is true but Statement (II) is false
(d) Statement (I) is false but Statement (II) is true

CHAPTER - 8
FET AND MOSFET

8.1 INTRODUCTION



$$\omega_{dep} = \left[\frac{2\in}{q}\left[\frac{1}{N_A}+\frac{1}{N_B}\right]\left[v_{bi}+v_R\right]^{Y_2}\right]^{1/2}$$

ω_{dep} = Basic depletion with standard formula
v_{bi} = Built in potential or contact potential

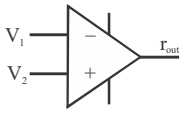
$$v_{bi} = V_T \ln\left[\frac{N_A N_D}{n_i}\right]$$

v_R = applied reverse biased

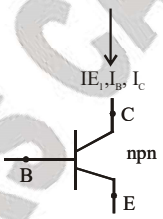
8.1.1 Field Effect Transistor is an unpolar device

1. JFET-n-type and p-type
2. MOSFET
(i) Depletion type MOSFET-n type and p type
(ii) Depletion Enhancement type MOSFET-n type and p type

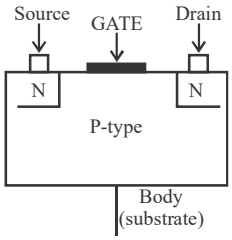
Operational Amplifier



BJT Amplifier



FET Amplifier



3. FET is a unipolar device because the current conduct only due to majority carrier this is known as the field effect transistor.
4. It is field effect transistor that is in which current is controlled by electric field and there is not leakage current and it is less noisy as compared to BJT.
5. Source, Drain and Gate are these Basic terminal of any FET device.

8.1.2 Source

It is the terminal through which majority carriers enter the bar-since carrier come from it ie why is called as source.

8.1.3 Drain

It is the terminal through which majority carrier leaves the channel. They are drain out from this terminal.

GATE QUESTIONS

1. An n-channel enhancement mode MOSFET is biased at VBS > VTH and VDSD > (VBS – VTH), where VGS is the gate to source voltage, VDS is the drain to source voltage and VTH is the threshold voltage. Considering channel length modulation effect to be significant, the MOSFET behaves as a

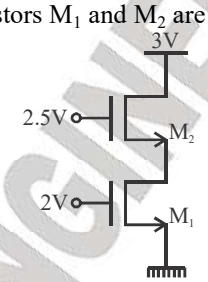
[GATE - 2017]

(a) Voltage source with zero output impedence
(b) Voltage source with non-zero output impedence
(c) Current source with finite output impedence
(d) Current source with infinite output impedence

2. A MOS capacitor is fabricated on p-type Si (silicon) where the metal work function is 4.1eV and electron affinity of Si is 4.0eV, $E_C - E_F$ = 0.9eV; where E_C and E_F are conduction band minimum and the Fermi energy levels of Si, respectively. Oxide $\varepsilon_r = 3.9$, $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm, oxide thickness $t_{ox} = 0.1\mu m$ and electron charge $q = 1.6 \times 10^{-19}$ C. If the measured flat band voltage of this capacitor is –1V, then the magnitude of the fixed charge at the oxide semiconductor interface, in nC/cm+, is _____.

[GATE - 2017]

3. Assuming that transistors M_1 and M_2 are identical and have a threshold voltage of 1V, the state of transistors M_1 and M_2 are respectively



[GATE - 2017]

(a) Saturation, Saturation
(b) Linear, Linear
(c) Linear, Saturation
(d) Saturation, Linear

4. In the circuit shown, transistor Q_1 and Q_2 are biased at a collector current of 2.6mA. Assuming the transistor current gains are sufficiently large to assume collector current equal to emitter current and thermal voltage of 26mV, the magnitude of voltage gain V_0/V_s in the mid band frequency range is _____ (up to second decimal place).

[GATE - 2017]

5. Consider the following statements for a metal oxide semiconductor field after effect transistor (MOSFET)

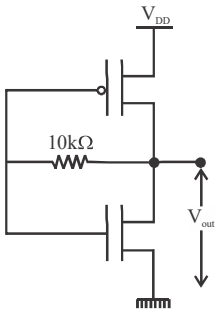
P: As channel length reduces, OFF-state current increases
Q: As channel length reduces, output resistance increases
R: As channel length reduces, threshold voltage remains constant
S: As channel reduces, ON current increases

Which of the above statements are INCORRECT?

[GATE - 2017]

(a) P and Q (b) P and S
(c) Q and R (d) R and S

6. What is the voltage V_{out} in the following circuit?



[GATE - 2017]

SOLUTIONS

Sol. 1. (c)
If the effect of channel length modulation is considered then the output resistance is finite value.

Sol. 2. (6.903)

So ϕsemiconductor = 4 + 0.9
= 4.9ev
{Work function $\Rightarrow E_{Vacuum} - E_{fermilevel}$}

$$V_{FB} = \phi_{ms} - \frac{q_{ox}}{C_{ox}}$$

$$-1 = -0.8 - \frac{q_{ox}}{C_{ox}}$$

$\begin{cases} V_{FB} \rightarrow \text{Flat band voltage} \\ \phi_{ms} \rightarrow \phi_m - \phi_s \end{cases}$

$\begin{cases} \frac{q_{ox}}{C_{ox}} \Rightarrow \text{potential developed due to charge at surface} \end{cases}$

$$0.2 = \frac{q_{ox}}{C_{ox}}$$

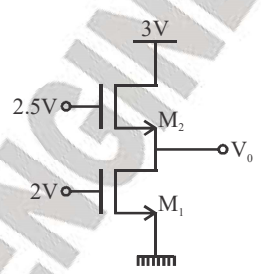
$q_{ox} = 0.2\ C_{ox}$

$$= 0.2\frac{\varepsilon_{ox}}{t_{ox}}$$

$$= 0.2 \times \frac{3.9 \times 8.85 \times 10^{-14}}{10^{-5}}$$

$q_{ox} = 6.903\ nC/cm^2$

Sol. 3. (c)



Given $V_{th} = 1V$

Here both the transistors are 'ON'
For M_2:
$V_G - V_{th} < V_D$ [1.5 < 3]
$\Rightarrow M_2$ is in saturation
For M_1:
Let us assume M_1 is in saturation
$(I_D)M_2 = (I_D)M_1$
$(2.5 - V_0 - 1)^2 = (2 - 1)^2$ [$\because I_D \propto (V_{GS} - V_{th})^2$]
$\therefore V_0 = 0.5$
$V_{GS} - V_{th} > V_{DS}$ [1 > 0.5]
$\Rightarrow$ out assumption is wrong
$\therefore M_1$ is in triode region
$M_2 \rightarrow$ saturation
$M_1 \rightarrow$ triode

Sol. 4. (50)

Sol. 5. (c)
P: TRUE
Q: FALSE: As channel length reduces, output resistance reduces
R: As channel length reduces, threshold voltage reduces
S: TRUE

Sol. 6. (b)

Sol. 7. (2 mA)

$$V_G = 8 \times \frac{5}{5+3} = 5V$$

$$V_s = I_D \cdot 1k\Omega$$

$$V_{GS} = 5 - I_D\ 1k\Omega$$

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{tn})^2$$

$$I_D = \frac{1}{2} \times 10^{-3}(5 - I_D.1k - 1)^2$$

$$2000I_D = (4 - I_D.1k)^2$$

$$2000I_D = 16 + I_D^2.10^6 - 8I_D.1k$$

$$10^6 I_D^2 - 10^4 I_D + 16 = 0$$

ESE OBJ QUESTIONS

1. When the drain voltage in an n- MOSFET is negative, it is operating in

[EE ESE - 2015]

(a) Active region (b) Inactive region
(c) Ohmic region (d) Reactive region

2. Consider the following statements regarding a differential amplifier using an FET pair , the differential output offset voltage is due to
1. Mismatch between FET parameters
2. Difference between the values of resistors used in the circuit even through they are marked nominally equal
3. Variation in the operating voltage of the circuit
Which of the above statements are correct ?

[EE ESE - 2014]

(a) 1, 2 and 3 (b) 2 and 3 only
(c) 1 and 3 only (d) 1 and 2 only

3. Statement (I): MOSFET's are intrinsically faster than bipolar devices
Statement (II): MOSFETs have excess minority carrier

[EE ESE - 2013]

(a) Both statement(I) and statement (II) are individually true and statement (II) is the correct explanation of statement (I)
(b) Both statement(I) and statement (II) are individually true but statement (II) is not the correct explanation of statement (I)
(c) Statement (I) is true but statement (II) is false
(d) Statement (I) is false but statement (II) is true

4. The value of the capacity reactance obtainable from a reactance FET whose g_m is 12 rms when the gate-to-source resistance is 1/9 of the reactance of the gate-to-drain capacitor at frequency 5MHz is

[EE ESE - 2013]

(a) 650Ω (b) 750Ω
(c) 775 Ω (d) 800Ω

5. The following statements refer to an n-channel FET operated in the active region
1.The gate voltage V_{GS} reverse biases the junction
2.The drain voltage V_{DD} is negative with respect to the source
3.The current in the n channel is due to electrons
4. Increasing in the reverse bias V_{GS} increase the cross section for conduction

[EE ESE - 2013]

(a) 1 and 2 (b) 1 and 3
(c) 2 and 3 (d) 3 and 4

6. The regions of operation of MOSFET to work as a linear resistor and linear amplifier are

[EE ESE - 2013]

(a) Cut off and saturation respectively
(b) Triode cut off respectively
(c) Triode and saturation respectively
(d) Saturation and triode respectively

7. Statement (I): Most JFETs are designed to work in depletion mode
Statement (II): Depletion mode takes advantage of very high input resistance of reverse biased state

[EE ESE - 2012]

(a) Both statement(I) and statement (II) are individually true and statement (II) is the correct explanation of statement (I)
(b) Both statement(I) and statement (II) are individually true but statement (II) is not the correct explanation of statement (I)
(c) Statement (I) is true but statement (II) is false
(d) Statement (I) is false but statement (II) is true

GATE 2019

DIGITAL ELECTRONICS

ELECTRICAL ENGINEERING

ECG Publications

ECG Publications

A Unit of **ENGINEERS CAREER GROUP**

Head O ce: S.C.O-121-122-123, 2nd oor, Sector-34/A, Chandigarh-160022

Website: www.engineerscareergroup.in **Toll Free:** 1800-270-4242

E-Mail: ecgpublica ons@gmail.com | info@engineerscareergroup.in

GATE-2019: Digital Electronics| Detailed theory with GATE & ESE previous year papers and detailed solu ons.

First Edi on: 2016

Price of Book: *INR 510/-*

ECG PUBLICATIONS (A Unit of ENGINEERS CAREER GROUP) collected and proving data like: theory for di erent topics or previous year solu ons very carefully while publishing this book. If in any case inaccuracy or prin ng error may nd or occurred then **ECG PUBLICATIONS** (A Unit of ENGINEERS CAREER GROUP) owes no responsibility. The sugges ons for inaccuracies or prin ng error will always be welcome by us.

CONTENTS

CHAPTER - 1
NUMBER SYSTEM

1.1 DATA REPRESENTATION

Magnitude Representation	Complement Representation
1.Unsigned magnitude representation (positive): No sign bit **2.**Signed magnitude representation (positive, negative): One extra bit (sign) as MSB	**1.** (r–1)'s complement: (positive, negative) **2.** R's complement: (positive, negative) MSB = 0 (positive) MSB = 1 (negative)

1.1.1 Sign Magnitude Representation

"+" sign before a number indicate that it is positive (+ve) number and negative (–ve) sign before a number indicate that it is –ve number.

Replace +ve = 0 (MSB); –ve = 1 (MSB)

Example.

$(+1100101)_2 \rightarrow (01100101)_2$

$(+\ 101.001)_2 \rightarrow (0101.001)_2$

$(-10010)_2 \rightarrow (110010)_2$

$(-110.101)_2 \rightarrow (1110.101)_2$

1.1.2 Signed Representation

Ranges is identical as that of 1's complement is also has 2 unique representation for zero

Range = $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$

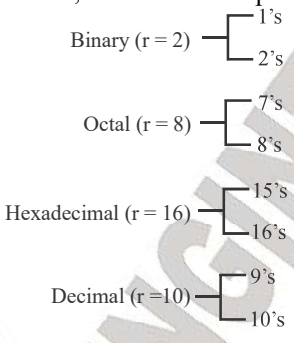
(n = 7): (– 63) to (+ 63)

1.1.3 Complement

There are two type of complements:

1. (r –1)'s complement
2. (r)'s complement

Where, r is base of complement



(r–1)'s complements: To determine the complement subtract the given no form maximum number possible in base.

GATE QUESTIONS

1. The number of bytes required to represent the decimal number 1856357 in packed BCD (Binary Coded Decimal) from is _____.

[GATE - 2014]

2. Which of the following is an invalid state in an 8-4-2-1 Binary coded decimal counter

[GATE - 2014]

(a) 1 0 0 0 (b) 1 0 0 1
(c) 0 0 1 1 (d) 1 1 0 0

3. The two numbers represented in signed 2's complement form are P=11101101 and Q=11100110. If Q is subtracted from P, the value obtained in signed 2's complement form is

[GATE - 2008]

(a) 100000111 (b) 00000111
(c) 11111001 (d) 111111001

4. X=01110 and Y=11001 are two 5-bit binary numbers represent in two's complement format. The sum of X and Y represented in two's complement format using 6 bit is :

[GATE - 2007]

(a) 100111 (b) 001000
(c) 000111 (d) 101001

5. The Octal equivalent of HEX and number AB.CD is

[GATE - 2007]

(a) 253.314 (b) 253.632
(c) 526.314 (d) 526.632

6. A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example the base-5 number 24 will be represented by its BCP code 010100. In the numbering system the BCP code 100010011001 corresponds to the following number in base –5 systems

[GATE - 2006]

(a) 423 (b) 1324
(c) 2201 (d) 4231

7. Decimal 43 in Hexadecimal and BCD number system is respectively

[GATE - 2005]

(a) B2, 0100 0011 (b) 2B, 0100 0011
(c) 2B, 0011 0100 (d) B2, 0100 0100

8. The range of signed decimal numbers that can be represented by 6-bite 1's complement number is

[GATE - 2004]

(a) –31 to +31 (b) –63 to +64
(c) –64 to +63 (d) –32 to +31

9. 11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number?

[GATE - 2004]

(a) 25, 9 and 57 respectively
(b) –6, –6 and –6 respectively
(c) –7, –7 and –7 respectively
(d) –25, –9 and –57 respectively

10. –bit 2's complement representation of a decimal number is 1000. The number is

[GATE - 2002]

(a) +8 (b) 0
(c) –7 (d) –8

11. The 2's complement representation of –17 is

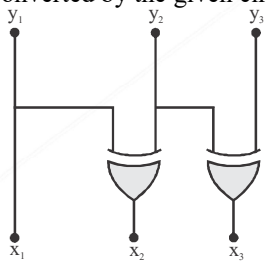
[GATE - 2001]

(a) 01110 (b) 01111
(c) 11110 (d) 10001

ASSIGNMENT

1. When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero?
(a) Sign magnitude
(b) 1's complement
(c) 2's complement
(d) 9's complement

2. In the following codes a binary number $Y_1Y_2Y_3$ is converted by the given circuit.



(a) Excess-3 Code (b) Gray Code
(c) Decimal Code (d) BCD Code

3. Addition of all the gray code to convert decimal (0-9) into gray code is:
(a) 129 (b) 108
(c) 69 (d) 53

4. Input

(a) + 255 (b) +127
(b) +31 (d) Zero

5. If $(123)_5 = (X3)_Y$, then the number of possible values of X is
(a) 4 (b) 3
(c) 2 (d) 1

6. A computer has the following negative numbers stored in binary form as shown. The wrongly stored number is:
(a) –37 as 11011011
(b) –89 as 10100111
(c) –48 as 11101000
(d) –32 as 11100000

7. Octal equivalent of hexadecimal AFAFAF is
(a) 53276757 (b) 76727673
(c) 53727657 (d) 76727672

8. $(177)_8 + 1 = (X)_8$, the value of x is
(a) 178 (b) 179
(c) 200 (d) None of these

9. Noting that $3^2=9$, formulate a simple procedure for converting base–3 numbers directly to base –9 use the procedure to convert $(2110201102220112)_3$ to base 9.
(a) $(66582614)_9$
(b) $(2206112414)_9$
(c) $(73642815)_9$
(d) None of these

10. Identify the first 10 decimal digits in Base 4 number system
(a) 0, 1, 2, 3, 4, 5, 6, 0, 1, 2
(b) 0, 1, 2, 3, 4, 5, 6, 7, 0, 1
(c) 0, 1, 2, 3, 10, 11, 12, 13, 14
(d) 0, 1, 2, 3, 10, 11, 12, 13, 20, 21

11. What is the 11's complement of $(935)_{12}$?
(a) 124_{11} (b) 234_{10}
(c) 286_{12} (d) 330_{10}

12. X and Y are successive digits in a positional number system. Also $XY = 25_{10}$ and $YX = 31_{10}$. Determine the Radix value of the system and value of X and Y.
(a) 6, 4, 2 (b) 7, 3, 4
(c) 7, 4, 3 (d) 6, 4, 3

13. Consider the signed Binary numbers A = 01000110 and B = 11010011, where B is in 2's complement from. Match the following.

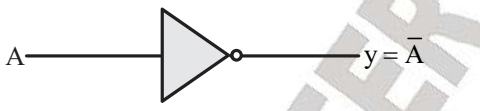
List-I	List-II

CHAPTER - 2
LOGIC GATES & BOOLEAN ALGEBRA

2.1 LOGIC GATE

1.The fundamental building block of digital system. Logic gate means that output and input pattern of gate are assigned logically.
2.The inter connection of Gate to perform a variety of logical operation is called logic design.
3.The input and output of logic gate can occur only in two levels. These level are termed as high (1) and Low (0) simply.
4.Truth table show how the logic circuit o/p respond to various combination of logic level of i/p.
There are various types of gates:
(i)Basic Gates: NOT, AND & OR
(ii)Universal Gate: NAND & NOR
(iii)EXOR & ENOR: Arithmetic, comparator, code converter, parity generator and parity checker.

1. NOT Gate



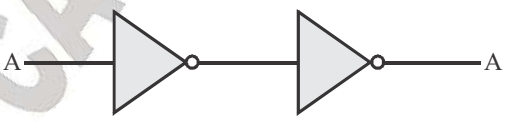
Truth Table

A	y
0	1
1	0

(i)

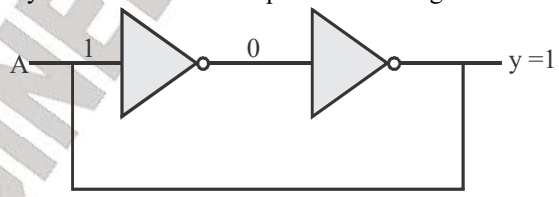
Switching Diagram

(ii)



Buffer Storage

(iii) It act as basic memory element or cross coupled latch storage element

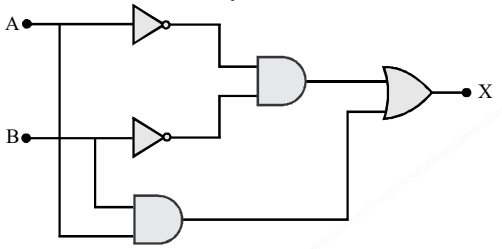


Basic Memory Element

Or mostly represented as

GATE QUESTIONS

1. A and B are the logical inputs and X is the logical output shown in the figure. The output X is related to A and B by



[GATE - 2017]

(a) $X = \overline{A}B + \overline{B}A$ (b) $X = AB + \overline{B}A$

(c) $X = AB + \overline{A}\,\overline{B}$ (d) $X = \overline{A}\,\overline{B} + \overline{B}A$

2. Figure 1 shows a 4-bit ripple carry adder realized using full adders and figure 2 shows the circuit of a full adder (FA). The propagation delay of the XOR, AND and OR gates in figure 2 are 20ns, 15ns and 10 ns, respectively. Assume all the inputs to the 4-bit adder are initially reset to 0.

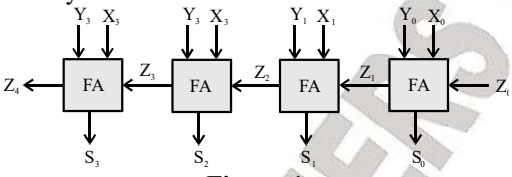


Figure-1

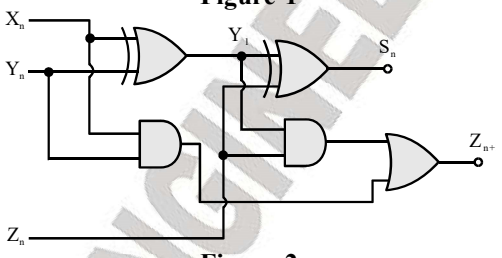
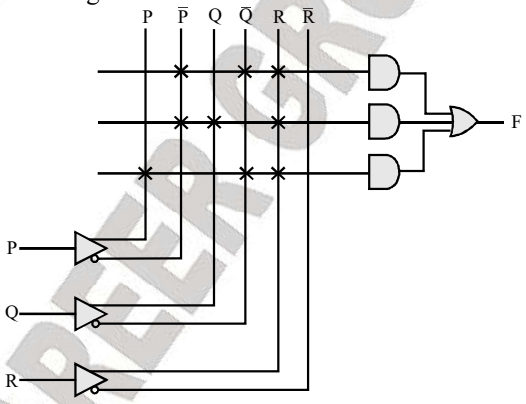


Figure-2

At t = 0, the inputs to the 4-bit adder are changed to $X_3X_2X_1X_0$ = 1100, $Y_3Y_2Y_1Y_0$ = 0100 and Z_0 = 1. The output of the ripple carry adder will be stable at t (in ns) = _____

[GATE - 2017]

3. A programmable logic array (PLA) is shown in the figure.



The Boolean function F implemented is

[GATE - 2017]

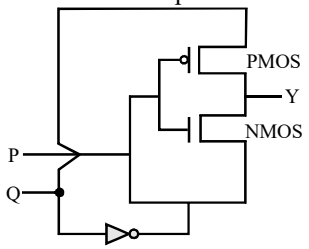
(a) $\overline{P}\,\overline{Q}R + \overline{P}QR + P\overline{Q}\,\overline{R}$

(b) $(\overline{P}+\overline{Q}+R)(\overline{P}+Q+R+(P+\overline{Q}+\overline{R})$

(c) $\overline{P}\,\overline{Q}R + \overline{P}QR + P\overline{Q}\,\overline{R}$

(d) $(\overline{P}+\overline{Q}+R)(\overline{P}+Q+R)+(P+\overline{Q}+\overline{R})$

4. For the circuit shown in figure, P and Q are the inputs and Y is the output.



The logic implemented by the circuit is

[GATE - 2017]

CHAPTER - 3
COMBINATIONAL IC'S

3.1 INTRODUCTION

1.Gates are available as SSI′s.
2.Adder, Multiplexer, Comparators and Encoder's are available in MSI.
3.SSI gates are mainly used for realizing simple Logic functions normally encountered in inter-counting.

3.1.1 Sequential logic

Logic circuits whose output are determined by the sequence in which input signals are applied

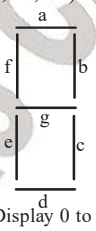
3.1.2 Glitch

A momentry (short pulse) Duration pulse.
For any logic Design it is always essential to design a product which meets the requirement as:
1. Minimum cost
2. Minimum space requirement
3. Maximum speed of operation
4. Easy availability of component
5. Ease of inter connection of component
6. Easy to Design

Example.

Basic Tool used in combinational circuit analysis is Karnaugh map (k-Map)
If we design this display by 4 bit then form (0 to 9) = BCD code valid and A to F (all status are invalid)

$$f(A,B,C,D) = \sum(0,1,2,3....9) + d\sum(10,11,12,13,14)$$



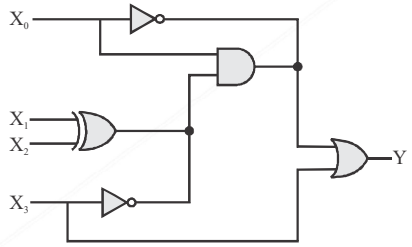
Display 0 to 9

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	x	x	x	x
10	1	1	x	x

$$f(A,B,C,D) = \bar{B} + \bar{C}\bar{D} + CD$$

GATE QUESTIONS

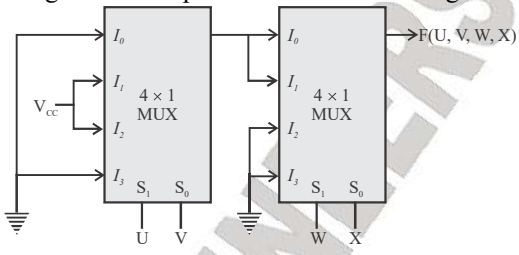
1. The logic gates shown in the digital circuit below use strong pull-down nMOS transistors for LOW logic level at the outputs. When the pull-downs are off, high-value resistors set the output logic levels to HIGH (i.e. the pull-ups are weak). Note that some nodes are intentionally shorted to implement "wired logic". Such shorted nodes will be HIGH only if the outputs of all the gates whose outputs are shorted are HIGH.



The number of distinct values $X_3\ X_2\ X_1\ X_0$ (out of the 16 possible values) that give Y = 1 is _____.

[GATE - 2018]

2. A four-variable Boolean function is realized using 4 × 1 multiplexes as shown in the figure.



The minimized expression for F(Uttar Pradesh V, W, X) is

[GATE - 2018]

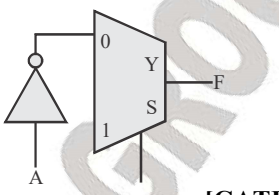
(a) $(UV+\bar{U}\bar{V})\bar{W}$

(b) $(UV+\bar{U}\bar{V})(\bar{W}\bar{X}+\bar{W}X)$

(c) $(U\bar{V}+\bar{U}V)\bar{W}$

(d) $(U\bar{V}+\bar{U}V)(\bar{W}\bar{X}+\bar{W}X)$

3. Consider the following circuit which uses a 2-to-1 multiplexer as shown in the figure below. The Boolean expression for output F in terms of A and B is

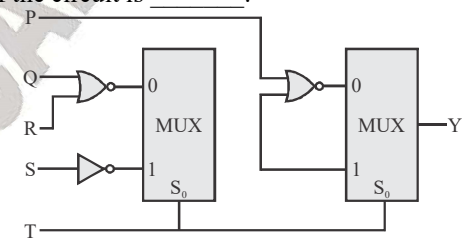


[GATE - 2016]

(a) A⊕B (b) $\overline{A+B}$

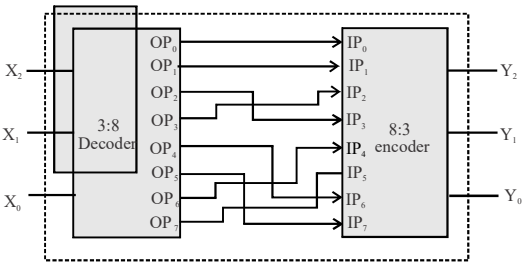
(c) A+B (d) $\overline{A \oplus B}$

4. For the circuit shown in figure, the delays of NOR gates, multiplexer and inverters are 2ns, 1.5ns and 1ns, respectively. If all the inputs P,Q,R,S and T are applied at the same time instant, the maximum propagation delay (in ns) of the circuit is _____.



[GATE - 2016]

5. Identify the circuit below

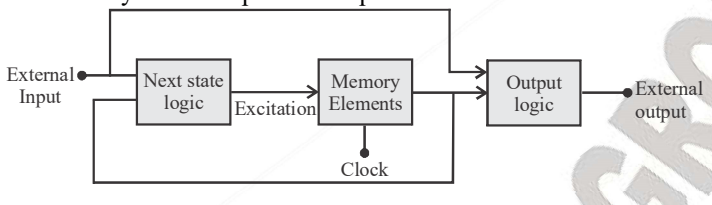


[GATE - 2016]

CHAPTER - 4
SEQUENTIAL LOGIC ANALYSIS

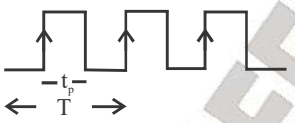
4.1 INTRODUCTION

In combinational circuit the present o/p depend only upon the present input any prior level. (Input condition) does not have any effect on present output.



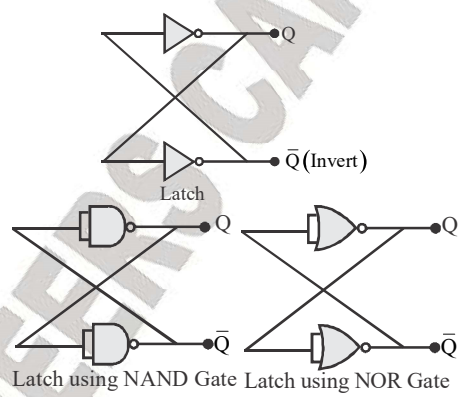
Next state depends upon next state logic and clock is used to receive & store data.

Timing Diagram



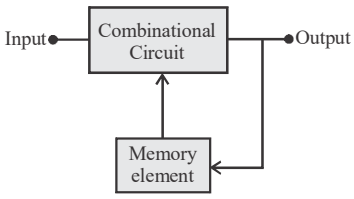
Where $t_p << T$

4.1.1 Bit Memory Cell



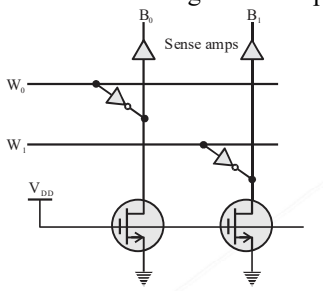
Bistable (MV) Latch Element (1 Bit memory device)

Block Diagram



GATE QUESTIONS

1. A 2 × 2 ROM array is built with the help of diodes as shown in the circuit below. Here W_0 and W_1 are signals that select the word lines and B_0 and B_1 are signals that are output of the sense amps based on the stored data corresponding to the bit lines during the read operation.



$$\begin{array}{c} \\ W_0 \\ W_1 \end{array}\begin{array}{c} \begin{array}{cc} B_0 & B_1 \end{array} \\ \begin{bmatrix} D_{00} & D_{01} \\ D_{10} & D_{11} \end{bmatrix} \end{array}$$

Bits stored in the ROM Array

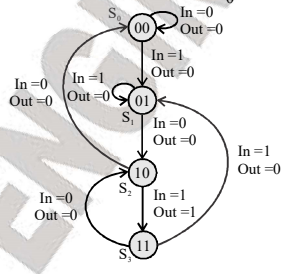
During the read operation, the selected word line goes high and the other word line is in a high impedance state. As per the implementation shown in the circuit diagram above, what are the bits corresponding to D_{ij} (where I = 0 or 1 and j = 0 or 1) stored in the ROM?

[GATE - 2018]

(a) $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$ (b) $\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$

(c) $\begin{bmatrix} 1 & 0 \\ 1 & 0 \end{bmatrix}$ (d) $\begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix}$

2. The state diagram of a finite state machine (FSM) designed to detect an overlapping sequence of three bits is shown in the figure. The FSM has an input 'In' and an output 'out'. The initial state of the FSM is S_0.

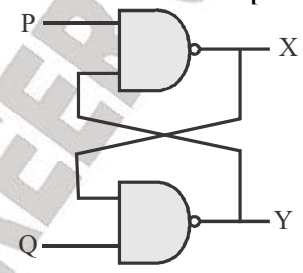


If the input sequence is 10101101001101, starting with the left most bit, then the number of times 'Out' will be 1 is ___

[GATE - 2017]

3. In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is: P = Q = '0', if the input condition is changed simultaneously to P = Q = '1', the outputs X and Y are

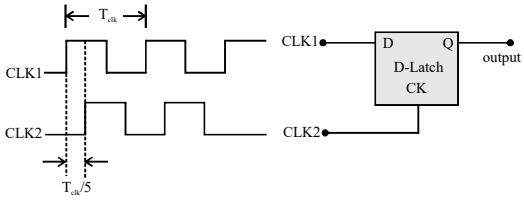
[GATE - 2017]



(a) X = '1', Y = '1'
(b) Either X = '1', Y = '0' or X = '0', Y = '1'
(c) Either X = '1' , Y = '1' or X = '0', Y = '0'
(d) X = '0', Y = '0'

4. Consider the D-latch shown in the figure, which is transparent when its clock input CK is high and has zero propagation delay. In the figure, the clock signal CLK1 has a 50% duty cycle and CLK2 is a one-fifth period delayed version of CLK1. The duty cycle at the output of the latch in percentage is _____.

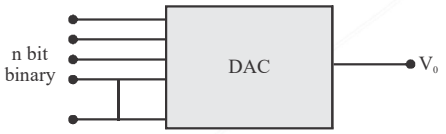
[GATE - 2017]



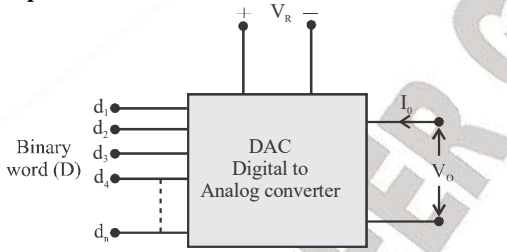
CHAPTER - 5
DIGITAL TO ANALOG CONVERTOR

5.1 DIGITAL TO ANALOG CONVERSION

1. It requires insulation of digital information to an equation analog information.
2. Usually refers as coding device.



Digital to analog convertor specification



5.1.1 Types of DAC

1. Weighted resister DAC
2. R-2R Ladder DAC

5.1.2 Parameter

1. Resolution
2. Analog output voltage
3. V_{Fs}
4. % resolution
5. Error / accuracy

5.1.3 General Equation

$$V_0 = k\{V_{Fs}\left(d_1 2^{-1} + d_2 2^{-2} + ... + d_n 2^{-n}\right)$$

Where, V_{FS} is full scale output voltage k is scaling factor usually "1".

d_1 is MSB with weight of $V_{Fs}/2$

d_n is LSB with weight of $V_{Fs}/2^n$

1. Resolution (D to A converter)

(i)Resolution of DAC is change in analog voltage corresponding to 1 bit LSB increment.

Step size = $\text{Resolution} = \frac{v_r}{2^n - 1}$

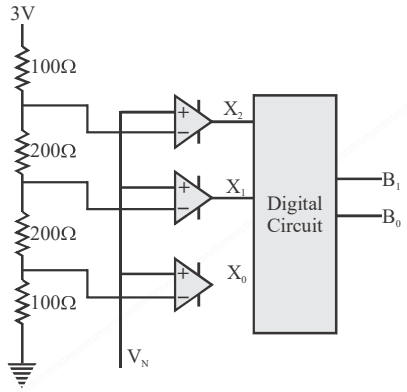
Where n is number of bit

v_r is reference voltage corresponding to logic 1.

(ii) It is smallest change in analog output.

GATE QUESTIONS

1. A 2-bit flash Analog to Digital Converter (ADC) is given below. The input is $0 \le V_N \le 3$ Volts. The expression for the LSB of the output B_0 as a Boolean function of X_2, X_1 and X_0 is

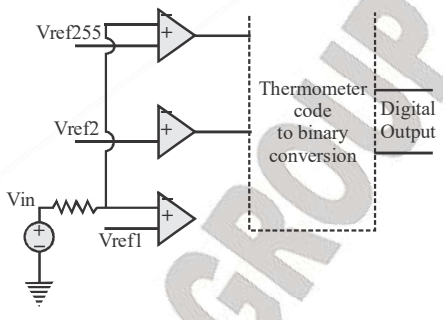


[GATE - 2016]

(a) $X_0[\overline{X_2 \oplus X_1}]$ (b) $\overline{X}_0[\overline{X_2 \oplus X_1}]$

(c) $X_0[X_2 \oplus X_1]$ (d) $\overline{X}_0[X_2 \oplus X_1]$

2. In an N bit flash ADC, the analog voltage is fed simultaneously to $2^N - 1$ comparators. The output of the comparators is then encoded to a binary format using digital circuit. Assume that the analog voltage source Vin (whose output is being converted to digital format) has a source resistance of 75Ω as shown in the circuit diagram below and the input capacitance of each comparator is 8pF. The input must settle to an accuracy of ½ LSB even for a full scale input change for proper conversion. Assume that the time taken by the thermometer to binary encoder is negligible.



If the flash ADC has 8 bit resolution, which one of the following alternatives is closest to the maximum sampling rate?

[GATE - 2016]

(a) 1 mega samples per second
(b) 6 mega samples per second
(c) 64 mega samples per second
(d) 256 mega samples per second

3. Consider a four bit D to A convener. The analog value corresponding to digital signals of values 0000 and 0001 are 0 V and 0.0625 V respectively. The analog value (in Volts) corresponding to the digital signal 1111 is____

[GATE - 2015]

4. Consider a four bit D to A convener the analog value corresponding to digital signals of values 0000 and 0001 are 0 V and 0.0625 V respectively. The analog value (in Volts) corresponding to the digital signal 1111 is _____.

[GATE - 2015]

5. If WL is the Word Line and BL the Bit Line, an SRAM cell is shown in

CHAPTER - 6
DIGITAL LOGIC FAMILIES

6.1 INTRODUCTION

1.Basically there are two types of semiconductor devices such as bipolar, unipolar, and based on these devices; integrated circuit (digital) have been made which are commercially available.

2.Various digital functions are being fabricated in a variety of form by using bipolar and unipolar technologies.

3.A group of (compatible IC's) with the same logic level and supply voltage for performing various logic families have been fabricated using a specific circuit configuration which is referred as logic family.

4.The various parameter or characteristics of digital IC's used to compare their performances are:

(i)Speed of operation
(ii)Power dissipation
(iii)Figure of Merit
(iv)Fan out
(v)Current/voltage parameter
(vi)Noise Immunity
(vii)Operating Temperature Range
(viii)Power supply Requirement
(ix)Flexibilities Available

6.2 THERE ARE TWO TYPES OF LOGIC FAMILIES

1.Bipolar Logic Family

(i) Saturated
(a) RTL(Resistor Transistor Logic)
(b) DCTL
(c) I^2L
(d) DTL
(e) TTL
(f) HTL

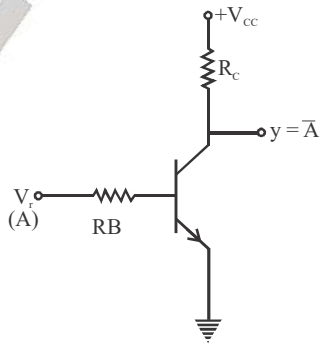
(ii)Unsaturated/Non-saturated
(a) Schottky TTL
(b) ECL(Emitter Coupled Logic)

2. Unipolar Logic Family

(i) MOS: MOSFET are employed in MOS Logic
(a)NMOS
(b)PMOS
(c)CMOS(Complementary Metal Oxide Semiconductor)
(d)BiCMOS uses CMOS for input and logic operation and Bipolar Devices for output.

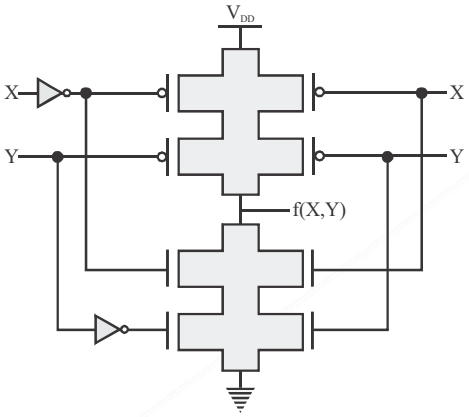
6.3 BASIC CONCEPTS OF LOGIC FAMILIES ANALYSES

Basic switching element:



GATE QUESTIONS

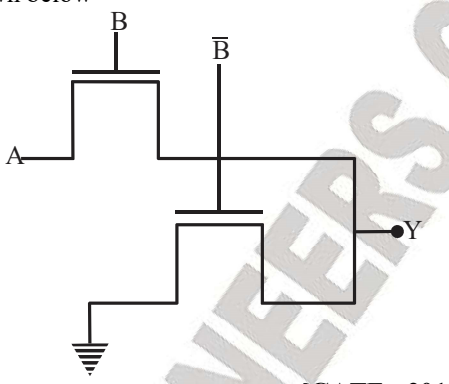
1. The logic f(X, Y) realized by the given circuit is



[GATE - 2018]

(a) NOR (b) AND
(c) NAND (d) XOR

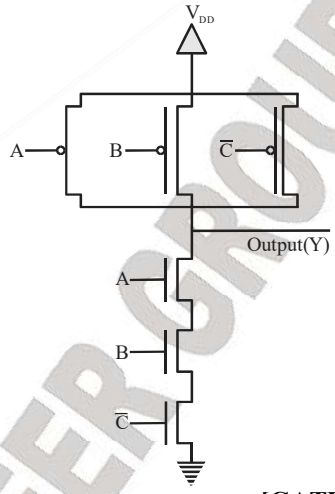
2. The logic functionality realized by the circuit shown below is



[GATE - 2016]

(a) OR (b) XOR
(c) NAND (d) AND

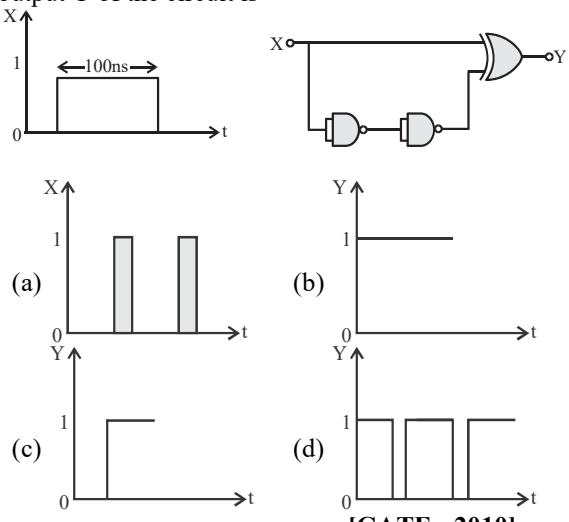
3. The output (Y) of the circuit shown in the figure is



[GATE - 2014]

(a) $\overline{A}+\overline{B}+C$ (b) $A+\overline{B}\cdot\overline{C}+A\cdot\overline{C}$
(c) $\overline{A}+B+\overline{C}$ (d) $A\cdot B\cdot\overline{C}$

4. The TTL circuit shown in the figure is fed with the waveform X (also shown). All gates have equal propagation delay of 10 ns. The output Y of the circuit is



[GATE - 2010]

ASSIGNMENT

1. Which has least power dissipation
(a) TTL (b) Schottky TTL
(c) CEL (d) CMOS

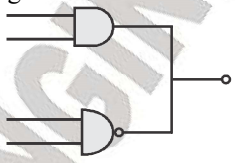
2. The TTL open collector output of two 2-input NAND gates are connected to a common pull-up resistor. If the inputs of the gates are A, B, C and D are respectively. The output is equal to
(a) $\overline{A \cdot B} \cdot \overline{C \cdot D}$ (b) $\overline{A \cdot B} + \overline{C \cdot D}$
(c) $A \cdot B + C \cdot D$ (d) $A \cdot B \cdot C \cdot D$

3. A three input NAND gates is used to be as an inverter. Which of the following measures will achieve better results?
(a)The two inputs not used are kept open
(b)The two inputs not used are connected to ground (0 level)
(c)The two inputs not used are (connected to supply V_{DD} (1 level)
(d)None of the above

4. For I_{OL}(max) = 16mA, I_{IL}(max) = 0.0016A, find out
(a) 16 (b) 10
(c) 1.6 (d) 100

5. The basic gate of ECL family is,
(a) NAND (b) NOR
(c) XOR (d) AND

6. Which one of the following logic functions is implemented by the gates when their open collector type outputs are tied together as shown in the given figure?



(a) $F = AB + C + D$ (b) $F = \overline{AB(C + D)}$
(c) F = AB + (C + D) (d) $F = \overline{AB + C + D}$

7. In which of the following option, the logic families are arranged in the decreasing order of Power dissipation?
(a) TTL, DTL, CMOS
(b) CMOS, TTL, DTL
(c) TTL, CMOS, DTL
(d) DTL, CMOS, TTL

8. In a standard TTL, totem pole refers to
(a) Multi emitter stage
(b) The phase splitter
(c) CMOS, TTL, DTL
(d) DTL, CMOS, TTL

9. In a standard TTL, totem pole refers to
(a) Multi emitter stage
(b) The phase splitter
(c) The output buffer
(d) Open collector output stage

10. In TTL floating input to a gate is considered
(a) Logical 0
(b) Logical 1
(c) Either 0 or 1
(d) Gate O/P will be undefined

11. The figure of merit of a logic is given by
(a)Gain bandwidth product
(b)Propagation delay and power dissipation product
(c)Fan out and propagation delay product
(d)Noise margin and power dissipation product

12. Match list-I with list-II and select the correct answer using the code given below in the list

List-I	**List-II**
A. HTL	(i)High fan out
B. CMOS	(ii)Highest speed of operation
C. I^2L	(iii)High noise immunity
D. ECL	(iv)Lowest product of power and delay

Codes: