GATE 2019

DIGITAL ELECTRONICS

ELECTRONICS ENGINEERING

ECG Publications

ECG Publications

A Unit of **ENGINEERS CAREER GROUP**

Head O ce: S.C.O-121-122-123, 2nd oor, Sector-34/A, Chandigarh-160022

Website: www.engineerscareergroup.in **Toll Free:** 1800-270-4242

E-Mail: ecgpublica ons@gmail.com | info@engineerscareergroup.in

GATE-2019: Digital Electronics| Detailed theory with GATE & ESE previous year papers and detailed solu ons.

First Edi on: 2016

Price of Book: *INR 510/-*

ECG PUBLICATIONS (A Unit of ENGINEERS CAREER GROUP) collected and proving data like: theory for di erent topics or previous year solu ons very carefully while publishing this book. If in any case inaccuracy or prin ng error may nd or occurred then **ECG PUBLICATIONS** (A Unit of ENGINEERS CAREER GROUP) owes no responsibility. The sugges ons for inaccuracies or prin ng error will always be welcome by us.

CONTENTS

CHAPTER - 1
NUMBER SYSTEM

1.1 DATA REPRESENTATION

Magnitude Representation	Complement Representation
1.Unsigned magnitude representation (positive): No sign bit **2.**Signed magnitude representation (positive, negative): One extra bit (sign) as MSB	**1.** (r–1)'s complement: (positive, negative) **2.** R's complement: (positive, negative) MSB = 0 (positive) MSB = 1 (negative)

1.1.1 Sign Magnitude Representation

"+" sign before a number indicate that it is positive (+ve) number and negative (–ve) sign before a number indicate that it is –ve number.

Replace +ve = 0 (MSB); –ve = 1 (MSB)

Example.

$(+1100101)_2 \rightarrow (01100101)_2$

$(+\ 101.001)_2 \rightarrow (0101.001)_2$

$(-10010)_2 \rightarrow (110010)_2$

$(-110.101)_2 \rightarrow (1110.101)_2$

1.1.2 Signed Representation

Ranges is identical as that of 1's complement is also has 2 unique representation for zero

Range = $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$

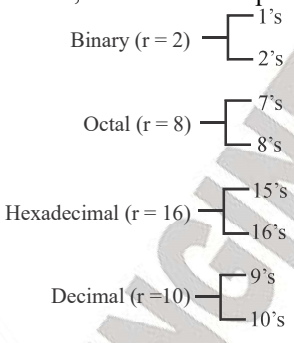
(n = 7): (– 63) to (+ 63)

1.1.3 Complement

There are two type of complements:

1. (r –1)'s complement
2. (r)'s complement

Where, r is base of complement

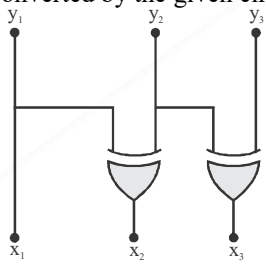


(r–1)'s complements: To determine the complement subtract the given no form maximum number possible in base.

ASSIGNMENT

1. When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero?
(a) Sign magnitude
(b) 1's complement
(c) 2's complement
(d) 9's complement

2. In the following codes a binary number $Y_1Y_2Y_3$ is converted by the given circuit.



(a) Excess-3 Code (b) Gray Code
(c) Decimal Code (d) BCD Code

3. Addition of all the gray code to convert decimal (0-9) into gray code is:
(a) 129 (b) 108
(c) 69 (d) 53

4. Input

(a) + 255 (b) +127
(b) +31 (d) Zero

5. If $(123)_5 = (X3)_Y$, then the number of possible values of X is
(a) 4 (b) 3
(c) 2 (d) 1

6. A computer has the following negative numbers stored in binary form as shown. The wrongly stored number is:
(a) –37 as 11011011
(b) –89 as 10100111
(c) –48 as 11101000
(d) –32 as 11100000

7. Octal equivalent of hexadecimal AFAFAF is
(a) 53276757 (b) 76727673
(c) 53727657 (d) 76727672

8. $(177)_8 + 1 = (X)_8$, the value of x is
(a) 178 (b) 179
(c) 200 (d) None of these

9. Noting that $3^2=9$, formulate a simple procedure for converting base–3 numbers directly to base –9 use the procedure to convert $(2110201102220112)_3$ to base 9.
(a) $(66582614)_9$
(b) $(2206112414)_9$
(c) $(73642815)_9$
(d) None of these

10. Identify the first 10 decimal digits in Base 4 number system
(a) 0, 1, 2, 3, 4, 5, 6, 0, 1, 2
(b) 0, 1, 2, 3, 4, 5, 6, 7, 0, 1
(c) 0, 1, 2, 3, 10, 11, 12, 13, 14
(d) 0, 1, 2, 3, 10, 11, 12, 13, 20, 21

11. What is the 11's complement of $(935)_{12}$?
(a) 124_{11} (b) 234_{10}
(c) 286_{12} (d) 330_{10}

12. X and Y are successive digits in a positional number system. Also $XY = 25_{10}$ and $YX = 31_{10}$. Determine the Radix value of the system and value of X and Y.
(a) 6, 4, 2 (b) 7, 3, 4
(c) 7, 4, 3 (d) 6, 4, 3

13. Consider the signed Binary numbers A = 01000110 and B = 11010011, where B is in 2's complement from. Match the following.

List-I	List-II

GATE QUESTIONS

1. The number of bytes required to represent the decimal number 1856357 in packed BCD (Binary Coded Decimal) from is _____.

[GATE - 2014]

2. Which of the following is an invalid state in an 8-4-2-1 Binary coded decimal counter

[GATE - 2014]

(a) 1 0 0 0 (b) 1 0 0 1
(c) 0 0 1 1 (d) 1 1 0 0

3. The two numbers represented in signed 2's complement form are P=11101101 and Q=11100110. If Q is subtracted from P, the value obtained in signed 2's complement form is

[GATE - 2008]

(a) 100000111 (b) 00000111
(c) 11111001 (d) 111111001

4. X=01110 and Y=11001 are two 5-bit binary numbers represent in two's complement format. The sum of X and Y represented in two's complement format using 6 bit is :

[GATE - 2007]

(a) 100111 (b) 001000
(c) 000111 (d) 101001

5. The Octal equivalent of HEX and number AB.CD is

[GATE - 2007]

(a) 253.314 (b) 253.632
(c) 526.314 (d) 526.632

6. A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example the base-5 number 24 will be represented by its BCP code 010100. In the numbering system the BCP code 100010011001 corresponds to the following number in base –5 systems

[GATE - 2006]

(a) 423 (b) 1324
(c) 2201 (d) 4231

7. Decimal 43 in Hexadecimal and BCD number system is respectively

[GATE - 2005]

(a) B2, 0100 0011 (b) 2B, 0100 0011
(c) 2B, 0011 0100 (d) B2, 0100 0100

8. The range of signed decimal numbers that can be represented by 6-bite 1's complement number is

[GATE - 2004]

(a) –31 to +31 (b) –63 to +64
(c) –64 to +63 (d) –32 to +31

9. 11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number?

[GATE - 2004]

(a) 25, 9 and 57 respectively
(b) –6, –6 and –6 respectively
(c) –7, –7 and –7 respectively
(d) –25, –9 and –57 respectively

10. –bit 2's complement representation of a decimal number is 1000. The number is

[GATE - 2002]

(a) +8 (b) 0
(c) –7 (d) –8

11. The 2's complement representation of –17 is

[GATE - 2001]

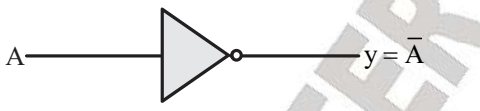
(a) 01110 (b) 01111
(c) 11110 (d) 10001

CHAPTER - 2
LOGIC GATES & BOOLEAN ALGEBRA

2.1 LOGIC GATE

1.The fundamental building block of digital system. Logic gate means that output and input pattern of gate are assigned logically.
2.The inter connection of Gate to perform a variety of logical operation is called logic design.
3.The input and output of logic gate can occur only in two levels. These level are termed as high (1) and Low (0) simply.
4.Truth table show how the logic circuit o/p respond to various combination of logic level of i/p.
There are various types of gates:
(i)Basic Gates: NOT, AND & OR
(ii)Universal Gate: NAND & NOR
(iii)EXOR & ENOR: Arithmetic, comparator, code converter, parity generator and parity checker.

1. NOT Gate



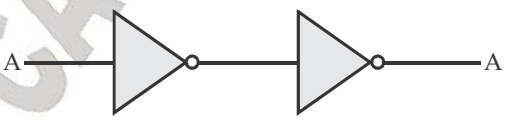
Truth Table

A	y
0	1
1	0

(i)

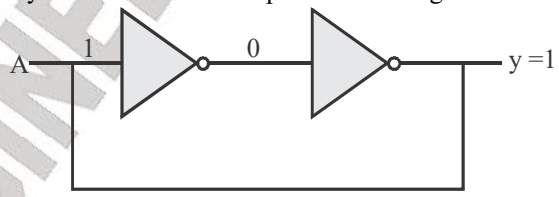
Switching Diagram

(ii)



Buffer Storage

(iii) It act as basic memory element or cross coupled latch storage element

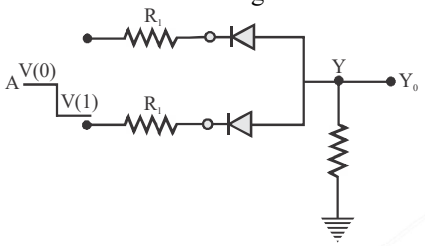


Basic Memory Element

Or mostly represented as

ASSIGNMENT

1. The circuit shown in the figure is:

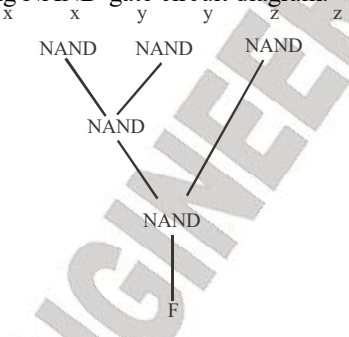


(a) Positive logic 'OR' circuit
(b) Negative logic 'OR' circuit
(c) Positive logic 'AND' circuit
(d) Negative logic 'AND' circuit

2. Which of the following logic expression is incorrect?
(a) $1 \oplus 0 = 1$ (b) $1 \oplus 1 \oplus 0 = 1$
(c) $1 \oplus 1 \oplus 1 = 1$ (d) $1 \oplus 1 = 0$

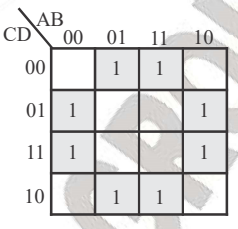
3. Which of the following Boolean algebra statements represent distributive law:
(a) (A+B) +C = A + (B+C)
(b) A. (B+C) = (A.B) + (A.C)
(c) A.(B.C) = (A.B).C
(d) None of these

4. Which expression is computed by the following NAND-gate circuit diagram.



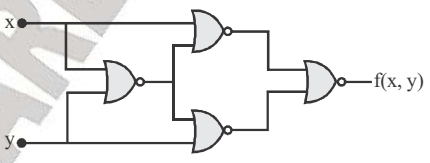
(a) X′Y′+Z (b) (X+Y) Z′
(c) X′Y′Z (d) X′+Y′+Z′

5. What is the equivalent Boolean expression in product of sum form for the K-map given below?



(a) BD′+B′D
(b) (B+C′+D) (B′+C+D′)
(c) (B+D′) (B′+D)
(d) (B′+D′) (B+D)

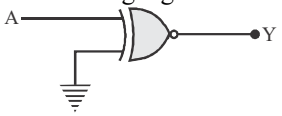
6. Identify the logic function performed by the circuit.



(a) Exclusive OR (b) Exclusive NOR
(c) NAND (d) NOR

7. The binary number 110011 is to be converted to gray code. The number of gates and type required are:
(a) 6, AND (b) 6, XNOR
(c) 6, XOR (d) 5, XOR

8. The output of the logic gate in the figure is

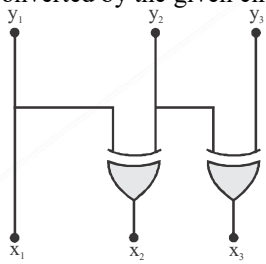


(a) AB + AC +BC (b) A + BC
(c) $\bar{A}$ (d) A + B + C

ASSIGNMENT

1. When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero?
(a) Sign magnitude
(b) 1's complement
(c) 2's complement
(d) 9's complement

2. In the following codes a binary number $Y_1Y_2Y_3$ is converted by the given circuit.



(a) Excess-3 Code (b) Gray Code
(c) Decimal Code (d) BCD Code

3. Addition of all the gray code to convert decimal (0-9) into gray code is:
(a) 129 (b) 108
(c) 69 (d) 53

4. Input

(a) + 255 (b) +127
(b) +31 (d) Zero

5. If $(123)_5 = (X3)_Y$, then the number of possible values of X is
(a) 4 (b) 3
(c) 2 (d) 1

6. A computer has the following negative numbers stored in binary form as shown. The wrongly stored number is:
(a) –37 as 11011011
(b) –89 as 10100111
(c) –48 as 11101000
(d) –32 as 11100000

7. Octal equivalent of hexadecimal AFAFAF is
(a) 53276757 (b) 76727673
(c) 53727657 (d) 76727672

8. $(177)_8 + 1 = (X)_8$, the value of x is
(a) 178 (b) 179
(c) 200 (d) None of these

9. Noting that $3^2=9$, formulate a simple procedure for converting base–3 numbers directly to base –9 use the procedure to convert $(2110201102220112)_3$ to base 9.
(a) $(66582614)_9$
(b) $(2206112414)_9$
(c) $(73642815)_9$
(d) None of these

10. Identify the first 10 decimal digits in Base 4 number system
(a) 0, 1, 2, 3, 4, 5, 6, 0, 1, 2
(b) 0, 1, 2, 3, 4, 5, 6, 7, 0, 1
(c) 0, 1, 2, 3, 10, 11, 12, 13, 14
(d) 0, 1, 2, 3, 10, 11, 12, 13, 20, 21

11. What is the 11's complement of $(935)_{12}$?
(a) 124_{11} (b) 234_{10}
(c) 286_{12} (d) 330_{10}

12. X and Y are successive digits in a positional number system. Also $XY = 25_{10}$ and $YX = 31_{10}$. Determine the Radix value of the system and value of X and Y.
(a) 6, 4, 2 (b) 7, 3, 4
(c) 7, 4, 3 (d) 6, 4, 3

13. Consider the signed Binary numbers A = 01000110 and B = 11010011, where B is in 2's complement from. Match the following.

List-I	List-II

ESE OBJ QUESTIONS

1. The addition of the two numbers $(1A8)_{16}$ + $(67B)_{16}$ will be:

[EC ESE - 2017]

(a) $(889)_{16}$ (b) $(832)_{16}$
(c) $(823)_{16}$ (d) $(723)_{16}$

2. The output of a NOR gate is:

[EC ESE - 2017]

(a) High if all of its inputs are high
(b) Low if all of its inputs are low
(c) High if all of its inputs are low
(d) High if only one of its inputs is low

3. What is the octal equivalent of $(5621.125)_{10}$?

[EE ESE - 2017]

(a) 1774.010 (b) 12765.100
(c) 16572.100 (d) 17652.010

4. What is the hexadecimal representation of $(657)_8$?

[EE ESE - 2017]

(a) 1 AF (b) D 78
(c) D 71 (d) 32 F

5. Given $(135)_{base\ x}$ + $(144)_{base\ x}$ = $(323)_{base\ x}$. What is the value of base x?

[EC ESE - 2014]

(a) 5 (b) 3
(c) 12 (d) 6

6. The number of one's present in the binary representation of
$15 \times 256 + 5 \times 16 + 3$ are

[EC ESE - 2014]

(a) 8 (b) 9
(c) 9 (d) 11

7. A seven-bit Hamming code is received as 1111101. What is the correct code?

[EC ESE - 2013]

(a) 1101111 (b) 1011111
(c) 1111111 (d) 1111011

8. Hexadecimal conversion of decimal number 227 will be:

[EC ESE - 2013]

(a) A3 (b) E3
(c) CC (d) C3

9. The decimal equivalent of binary number 10110.11 is:

[EC ESE - 2013]

(a) 16.75 (b) 20.75
(c) 16.50 (d) 22.75

10. The BCD code for a decimal number $(874)_{10}$ is:

[EC ESE - 2013]

(a) $(100001110100)_{BCD}$
(b) $(010001111000)_{BCD}$
(c) $(100001000111)_{BCD}$
(d) $(011110000100)_{BCD}$

11. Binary data is being represented in size of byte and in 2's complement form. The number of 0's present in representation of $(-127)_{decimal}$ is

[EC ESE - 2012]

(a) 8 (b) 7
(c) 6 (d) 5

12. If $(11X1Y)_8 = (12C9)_{16}$ then the values X and Y are

[EC ESE - 2012]

(a) 5 and 1 (b) 5 and 7
(c) 7 and 5 (d) 1 and 5

13. Statement (I): 2's complement arithmetic is preferred in digital computers.
Statement (II): The hardware required to obtain the 2's complement of a number, is simple.

[EE ESE - 2012]

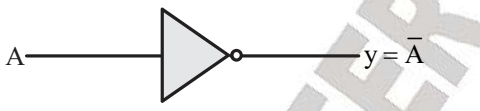
(a)Both statement (I) and statement (II) are individual true and statement (II) is the correct explanation of statement (I).

CHAPTER - 2
LOGIC GATES & BOOLEAN ALGEBRA

2.1 LOGIC GATE

1.The fundamental building block of digital system. Logic gate means that output and input pattern of gate are assigned logically.
2.The inter connection of Gate to perform a variety of logical operation is called logic design.
3.The input and output of logic gate can occur only in two levels. These level are termed as high (1) and Low (0) simply.
4.Truth table show how the logic circuit o/p respond to various combination of logic level of i/p.
There are various types of gates:
(i)Basic Gates: NOT, AND & OR
(ii)Universal Gate: NAND & NOR
(iii)EXOR & ENOR: Arithmetic, comparator, code converter, parity generator and parity checker.

1. NOT Gate



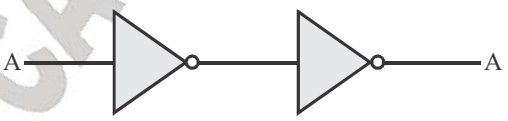
Truth Table

A	y
0	1
1	0

(i)

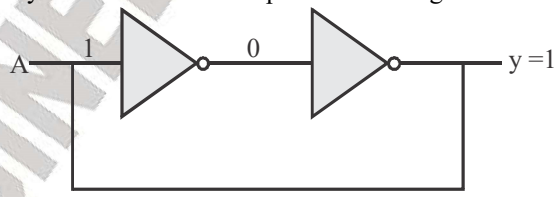
Switching Diagram

(ii)



Buffer Storage

(iii) It act as basic memory element or cross coupled latch storage element

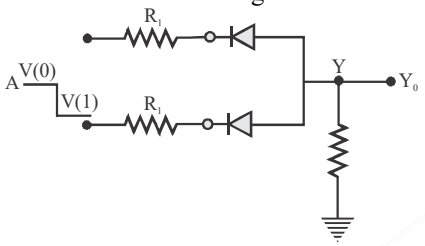


Basic Memory Element

Or mostly represented as

ASSIGNMENT

1. The circuit shown in the figure is:

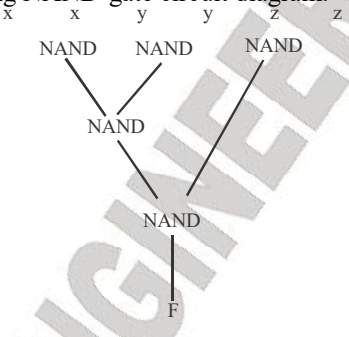


(a) Positive logic 'OR' circuit
(b) Negative logic 'OR' circuit
(c) Positive logic 'AND' circuit
(d) Negative logic 'AND' circuit

2. Which of the following logic expression is incorrect?
(a) $1 \oplus 0 = 1$ (b) $1 \oplus 1 \oplus 0 = 1$
(c) $1 \oplus 1 \oplus 1 = 1$ (d) $1 \oplus 1 = 0$

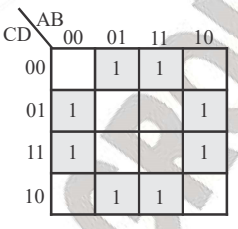
3. Which of the following Boolean algebra statements represent distributive law:
(a) (A+B) +C = A + (B+C)
(b) A. (B+C) = (A.B) + (A.C)
(c) A.(B.C) = (A.B).C
(d) None of these

4. Which expression is computed by the following NAND-gate circuit diagram.



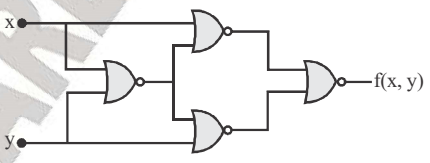
(a) X′Y′+Z (b) (X+Y) Z′
(c) X′Y′Z (d) X′+Y′+Z′

5. What is the equivalent Boolean expression in product of sum form for the K-map given below?



(a) BD′+B′D
(b) (B+C′+D) (B′+C+D′)
(c) (B+D′) (B′+D)
(d) (B′+D′) (B+D)

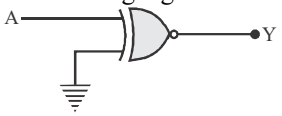
6. Identify the logic function performed by the circuit.



(a) Exclusive OR (b) Exclusive NOR
(c) NAND (d) NOR

7. The binary number 110011 is to be converted to gray code. The number of gates and type required are:
(a) 6, AND (b) 6, XNOR
(c) 6, XOR (d) 5, XOR

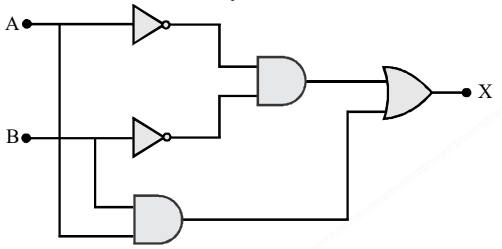
8. The output of the logic gate in the figure is



(a) AB + AC +BC (b) A + BC
(c) $\bar{A}$ (d) A + B + C

GATE QUESTIONS

1. A and B are the logical inputs and X is the logical output shown in the figure. The output X is related to A and B by



[GATE - 2017]

(a) $X = \overline{A}B + \overline{B}A$ (b) $X = AB + \overline{B}A$

(c) $X = AB + \overline{A}\,\overline{B}$ (d) $X = \overline{A}\,\overline{B} + \overline{B}A$

2. Figure 1 shows a 4-bit ripple carry adder realized using full adders and figure 2 shows the circuit of a full adder (FA). The propagation delay of the XOR, AND and OR gates in figure 2 are 20ns, 15ns and 10 ns, respectively. Assume all the inputs to the 4-bit adder are initially reset to 0.

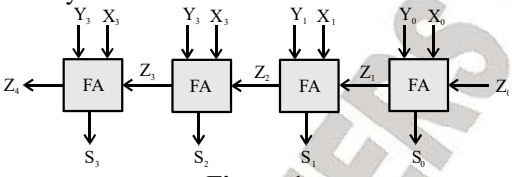


Figure-1

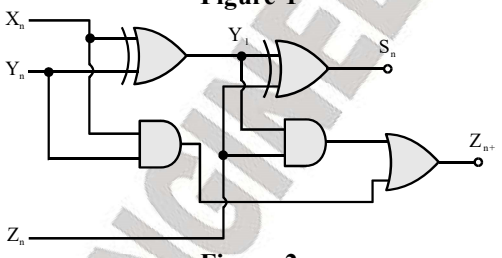
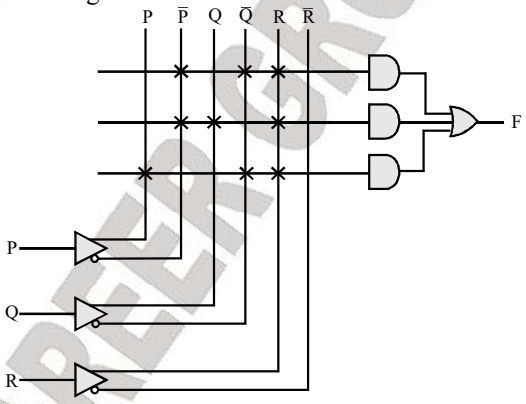


Figure-2

At t = 0, the inputs to the 4-bit adder are changed to $X_3X_2X_1X_0$ = 1100, $Y_3Y_2Y_1Y_0$ = 0100 and Z_0 = 1. The output of the ripple carry adder will be stable at t (in ns) = _____

[GATE - 2017]

3. A programmable logic array (PLA) is shown in the figure.



The Boolean function F implemented is

[GATE - 2017]

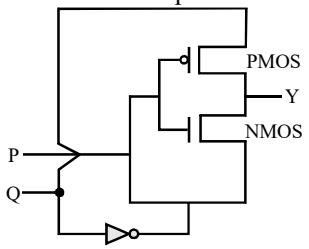
(a) $\overline{P}\,\overline{Q}R + \overline{P}QR + P\overline{Q}\,\overline{R}$

(b) $(\overline{P}+\overline{Q}+R)(\overline{P}+Q+R+(P+\overline{Q}+\overline{R})$

(c) $\overline{P}\,\overline{Q}R + \overline{P}QR + P\overline{Q}\,\overline{R}$

(d) $(\overline{P}+\overline{Q}+R)(\overline{P}+Q+R)+(P+\overline{Q}+\overline{R})$

4. For the circuit shown in figure, P and Q are the inputs and Y is the output.



The logic implemented by the circuit is

[GATE - 2017]

ESE OBJ QUESTIONS

1. A product of sums (POS) expression leads to what kind of logic circuit?

[EC ESE - 2018]

(a) OR – AND circuit
(b) NOR-NOR circuit
(c) AND-OR-INVERT circuit
(d) NAND – NAND circuit

2. If only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables, what is the maximum size of the multiplexer needed?

[EC ESE - 2017]

(a) 2^{n-2} line to 1 line
(b) 2^{n-1} line to 1 line
(c) 2^{n+1} line to 1 line
(d) 2^{n+2} line to 1 line

3. The simplification in minimal sum of product (SOP) of
Y = F(A, B,C,D)
$= \sum_m(0,2,3,6,7) + \sum(8,10,11,15)$
Using K-maps is

[EC ESE - 2017]

(a) $Y = AC + B\overline{D}$ (b) $Y = A\overline{C} + B\overline{D}$
(c) $Y = \overline{AC} + \overline{B}D$ (d) $Y = \overline{A}C + \overline{B}\overline{D}$

4. A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 is represented by 0001, ……, 9 by 1001. A combinational circuit is to be designed which takes 4 bits as input and output as 1, if the digit is ≥5, and 0 otherwise. If only AND, OR and NOT gates may be used, What is the minimum number of gates required?

[EC ESE - 2017]

(a) 4 (b) 3
(c) 2 (d) 1

5. How many 3 to 8 line decoders with an enabler input are needed to construct a 6 to 64 line decoder without using any other logic gates?

[EC ESE - 2017]

(a) 11 (b) 10
(c) 9 (d) 8

6. The minterm expansion of F(A, B,C) = $AB = B\overline{C} + A\overline{C}$ is

[EC ESE - 2017]

(a) $m_2 + m_4 + m_6 + m_1$
(b) $m_0 + m_1 + m_3 + m_5$
(c) $m_7 + m_6 + m_2 + m_4$
(d) $m_2 + m_3 + m_4 + m_5$

7. The logical expression, $AB\overline{C} + A\overline{B}C + A\overline{B}\overline{C}$.

[EE ESE - 2017]

(a) $\overline{A}(B + C)$ (b) $\overline{A} + \overline{B} + \overline{C}$
(c) $\overline{A}\overline{B}C$ (d) $A(\overline{C} + \overline{B})$

8. The logic function A + BC is the simplified from of which of the following?

[EE ESE - 2015]

(a) $AB + BC$ (b) $\overline{A}B + A\overline{B}C$
(c) $\overline{ABC}$ (d) $(A + B)(A + C)$

9. For a four variable K-Map, if each cell is assigned one integer value in range 0-15 then which is the cells adjacent to the cell corresponding to decimal value 7?

[EE ESE - 2015]

(a) 3, 5, 6 and 8 (b) 3, 5, 10 and 11
(c) 3, 5, 6 and 15 (d) 4, 6, 8 and 5

10. A binary-to-BCD encoder has four inputs D_0, C_0, B_0 and A_0 and five outputs D, C, B, A and VALID. The outputs D, C, B, A give the proper BCD value of the input and the VALID output is 1 if the input combination is a valid decimal code. If the input combination is an invalid decimal code, the VALID output becomes 0 and all of the D, C, B and A outputs show 0 values. If only NOT gates and 2-input

CHAPTER - 3
COMBINATIONAL IC'S

3.1 INTRODUCTION

1.Gates are available as SSI′s.
2.Adder, Multiplexer, Comparators and Encoder's are available in MSI.
3.SSI gates are mainly used for realizing simple Logic functions normally encountered in inter-counting.

3.1.1 Sequential logic

Logic circuits whose output are determined by the sequence in which input signals are applied

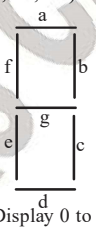
3.1.2 Glitch

A momentry (short pulse) Duration pulse.
For any logic Design it is always essential to design a product which meets the requirement as:
1. Minimum cost
2. Minimum space requirement
3. Maximum speed of operation
4. Easy availability of component
5. Ease of inter connection of component
6. Easy to Design

Example.

Basic Tool used in combinational circuit analysis is Karnaugh map (k-Map)
If we design this display by 4 bit then form (0 to 9) = BCD code valid and A to F (all status are invalid)

$$f(A,B,C,D) = \sum(0,1,2,3....9) + d\sum(10,11,12,13,14)$$



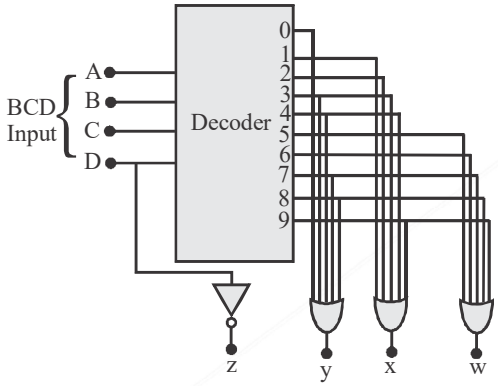
Display 0 to 9

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	x	x	x	x
10	1	1	x	x

$$f(A,B,C,D) = \bar{B} + \bar{C}\bar{D} + CD$$

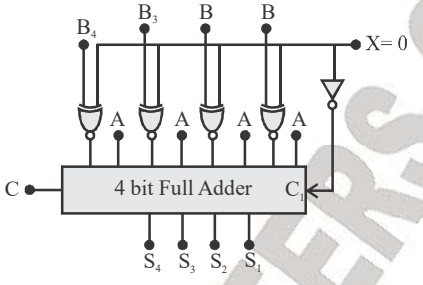
ASSIGNMENT

1. The following logic circuit (w, x, y, z) indicates



(a) Binary to BCD converter
(b) BCD to Binary converter
(c) BCD to Decimal converter
(d) BCD to EX – 3 converter

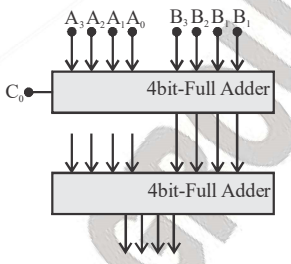
2. Identify the function of the following logic circuit



(a) 4-bit Binary adder
(b) 4-bit BCD Adder
(c) 4-bit Binary subtractor
(d) 4-bit BCD subtractor

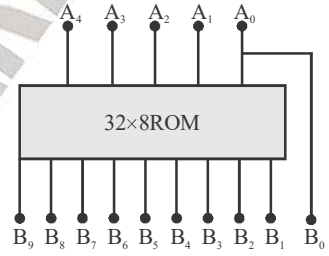
3. The following logic circuit adds two digits represented in the Excess-3 code. The correction required after adding the two digits in EX-3 from is as follows.
If $C_0 = 1$ and + 3

Identify the inputs to be given to the 2nd 4-bit full adder?



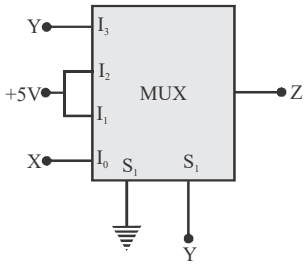
(a) C_0, C_0, 0, C_0 (b) 0, 0, C_0, C_0
(c) 0, 0, C_0, C_0 (d) $\overline{C}_0, \overline{C}_0, \overline{C}_0, 1$

4. The following circuit is used to implement circuit that generates the binary square of an input 5-bit number. What is the data stored in last location of ROM?



(a) 10101010 (b) 11001100
(c) 00110011 (d) 11110000

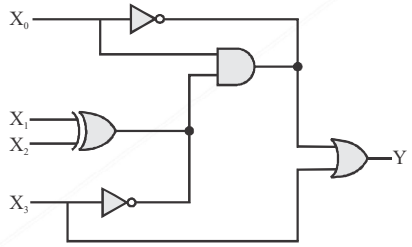
5. The output of the 4 × 1 multiplexer shown in figure is



(a) $X + Y$ (b) $\overline{X}\overline{Y} + X$
(c) $X\overline{Y}$ (d) $\overline{X} + \overline{Y}$

GATE QUESTIONS

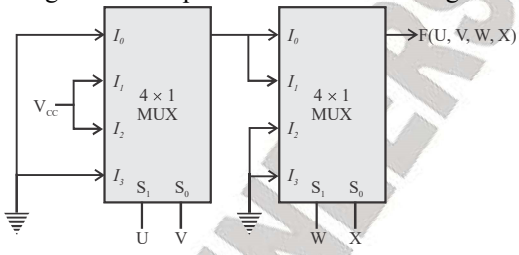
1. The logic gates shown in the digital circuit below use strong pull-down nMOS transistors for LOW logic level at the outputs. When the pull-downs are off, high-value resistors set the output logic levels to HIGH (i.e. the pull-ups are weak). Note that some nodes are intentionally shorted to implement "wired logic". Such shorted nodes will be HIGH only if the outputs of all the gates whose outputs are shorted are HIGH.



The number of distinct values $X_3\ X_2\ X_1\ X_0$ (out of the 16 possible values) that give Y = 1 is _____.

[GATE - 2018]

2. A four-variable Boolean function is realized using 4 × 1 multiplexes as shown in the figure.



The minimized expression for F(Uttar Pradesh V, W, X) is

[GATE - 2018]

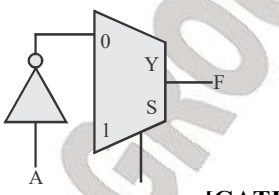
(a) $(UV+\bar{U}\bar{V})\bar{W}$

(b) $(UV+\bar{U}\bar{V})(\bar{W}\bar{X}+\bar{W}X)$

(c) $(U\bar{V}+\bar{U}V)\bar{W}$

(d) $(U\bar{V}+\bar{U}V)(\bar{W}\bar{X}+\bar{W}X)$

3. Consider the following circuit which uses a 2-to-1 multiplexer as shown in the figure below. The Boolean expression for output F in terms of A and B is

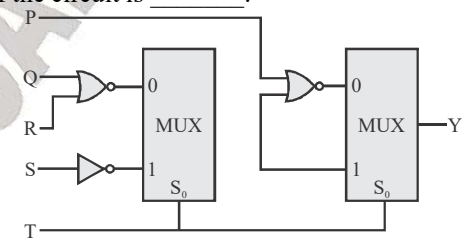


[GATE - 2016]

(a) A⊕B (b) $\overline{A+B}$

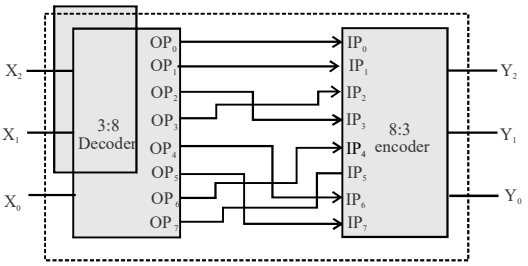
(c) A+B (d) $\overline{A \oplus B}$

4. For the circuit shown in figure, the delays of NOR gates, multiplexer and inverters are 2ns, 1.5ns and 1ns, respectively. If all the inputs P,Q,R,S and T are applied at the same time instant, the maximum propagation delay (in ns) of the circuit is _____.



[GATE - 2016]

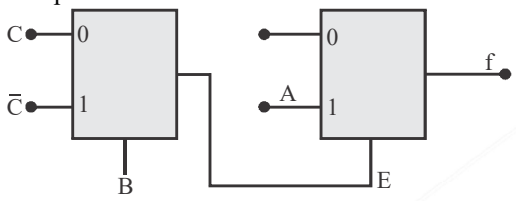
5. Identify the circuit below



[GATE - 2016]

ESE OBJ QUESTIONS

1. The Boolean function 'f' implemented as shown in the figure using two inputs multiplexers is



[EC ESE - 2014]

(a) $A\bar{B}C + AB\bar{C}$ (b) $ABC + A\bar{B}\bar{C}$
(c) $\bar{A}BC + \bar{A}B\bar{C}$ (d) $\bar{A}\bar{B}C + \bar{A}B\bar{C}$

2. A binary full-subtractor

[EC ESE - 2013]

(a)Consists of two cascaded half-subtractors
(b)Contains two half-subtractors and one OR gate
(c)Can subtract any binary number
(d)Can be made out of a full-adder

3. A digital multiplexer can be used for:
1. Parallel to serial conversion
2. Many-to-one switch
3. Generating memory chip select
4. Code conversion

[EC ESE - 2013]

(a) 1, 2 and 3 (b) 2 and 3 only
(c) 1 and 2 only (d) 1 and 3 only

Direction: The following items consists of two statements, one labeled as 'Statement (I)' and the other as 'Statement (II)'. You are to examine these two statements carefully and select the answers to these items using the code given below:
(a)Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I).
(b)Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I).
(c)Statement (I) is true but Statement (II) is false.
(d)Statement (I) is false but Statement (II) is true.

4. Statement (I): The carry look-ahead adder is fast adder.
Statement (II): The carry look-ahead adder generates the carry and the sum digits directly.

[EC ESE - 2012]

(a)Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I).
(b)Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I).
(c)Statement (I) is true but Statement (II) is false.
(d)Statement (I) is false but Statement (II) is true.

5. The logic function;
Out = ab + bc + ca defines
1. The output of 3-input XOR gate
2. The output of 1 3-input majority gate
3. The sum output of a full adder
4. The carry output of a full adder
Which of these statements are correct?

[EC ESE - 2011]

(a) 1 and 3 (b) 2 and 3
(c) 3 and 4 (d) 2 and 4

6. Assertion (A): A de-multiplexer cannot be used as a decoder.
Reason (R): A de-multiplexer selects one of many outputs, whereas a decoder selects an output corresponding to the coded input.

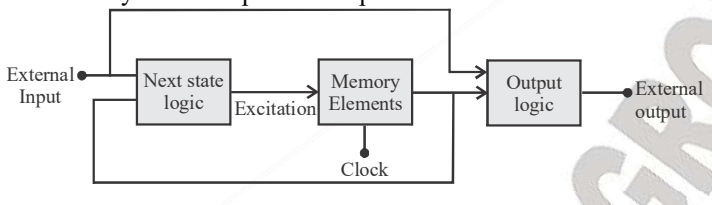
[EC ESE - 2011]

(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is not a correct explanation of A
(c) A is true but R is false

CHAPTER - 4
SEQUENTIAL LOGIC ANALYSIS

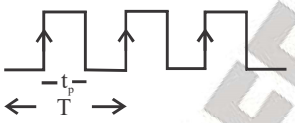
4.1 INTRODUCTION

In combinational circuit the present o/p depend only upon the present input any prior level. (Input condition) does not have any effect on present output.



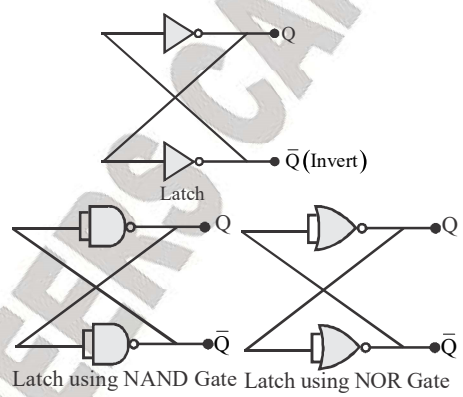
Next state depends upon next state logic and clock is used to receive & store data.

Timing Diagram



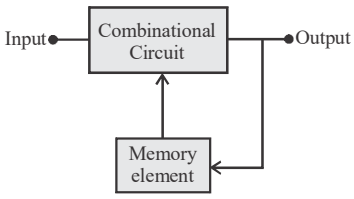
Where $t_p << T$

4.1.1 Bit Memory Cell



Bistable (MV) Latch Element (1 Bit memory device)

Block Diagram



ASSIGNMENT

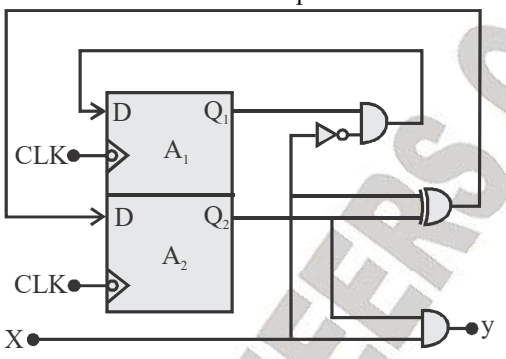
1. A 4-bit register converts the binary stored in the register to its 2′s complement value when input x = 1. This FFS used are T-FFS. Determine the inputs of flip-flops i.e. T_A, T_B, T_C, T_D.

(a) 0, 1, (A + B)x, $\bar{A}x$
(b) (B + C + D)x, (C + D)x, Q_D, x_0
(c) $1, 0x, (C+D)x, \overline{(C+D)}x$
(d) $(B+C)\bar{x}, (C+D)x, D\bar{x}, 0$

2. A counter, constructed using T-FFS, counts the decimal digits according to 2, 4, 2, 1 code. The input T_B is

(a) A′ B + CD (b) A′ B + BCD
(c) A′ B + D (d) A′ B + A′ D

3. A sequential circuit is as shown below. If present states of A_1, A_2, are 1, 0 and x = 1, what is its next state and output

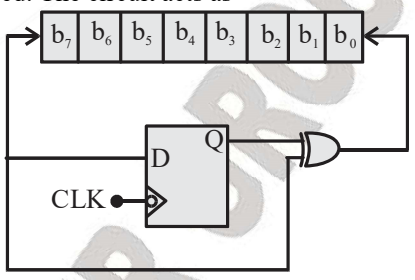


(a) 0, 1, 0 (b) 1, 0, 0
(c) 0, 1, 1 (d) 1, 1, 1

4. In a 4 bit modulo-6 ripple counter the proportional delay of J-K Flip flop is 50ns. What is the max clock frequency that can used without skipping a count.

(a) 2MHz (b) 4 MHz
(c) 5 KHz (d) 5 MHz

5. In the following logic circuit, the 8 bit left shift register and D-Flip flop is synchronized with same clock. The D-Flip flop is initially cleared. The circuit acts as



(a) Binary to 2′s comp converter
(b) Binary to EX-3 code converter
(c) Binary to 1′s comp converter
(d) Binary to Gray code converter

6. A N-bit register is constructed using D-flip-flops. Match the following List- I with List- II

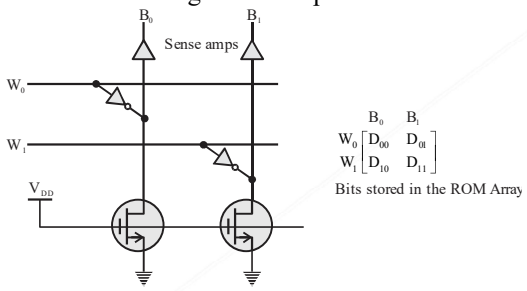
List-I	**List-II**
A.Parallel in parallel out	(i)(2N-1) clock pulses
B.Serial in serial out	(ii)One clock pulses
C.Parallel in serial out	(iii)N clock pulses
D.Serial in parallel out	(iv)(N-1) clock pulses

Codes:
(a) A-iii, B-iv, C-ii, D-i
(b) A-iv, B-ii, C-i, D-iii
(c) A-iii, B-ii, C-iv, D-i
(d) A-ii, B-i, C-iv, D-iii

7. Determine the output of the negative Edge triggered J-K flip flop for the following input waveforms at T_1, T_2, T_3, T_4. Assume the hold time FF is 0.

GATE QUESTIONS

1. A 2 × 2 ROM array is built with the help of diodes as shown in the circuit below. Here W_0 and W_1 are signals that select the word lines and B_0 and B_1 are signals that are output of the sense amps based on the stored data corresponding to the bit lines during the read operation.



$$\begin{array}{c} \\ W_0 \\ W_1 \end{array}\begin{array}{c} \begin{array}{cc} B_0 & B_1 \end{array} \\ \begin{bmatrix} D_{00} & D_{01} \\ D_{10} & D_{11} \end{bmatrix} \end{array}$$

Bits stored in the ROM Array

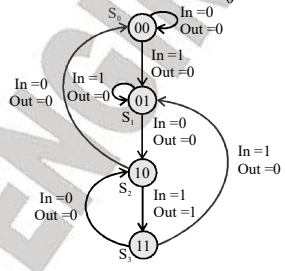
During the read operation, the selected word line goes high and the other word line is in a high impedance state. As per the implementation shown in the circuit diagram above, what are the bits corresponding to D_{ij} (where I = 0 or 1 and j = 0 or 1) stored in the ROM?

[GATE - 2018]

(a) $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$ (b) $\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$

(c) $\begin{bmatrix} 1 & 0 \\ 1 & 0 \end{bmatrix}$ (d) $\begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix}$

2. The state diagram of a finite state machine (FSM) designed to detect an overlapping sequence of three bits is shown in the figure. The FSM has an input 'In' and an output 'out'. The initial state of the FSM is S_0.

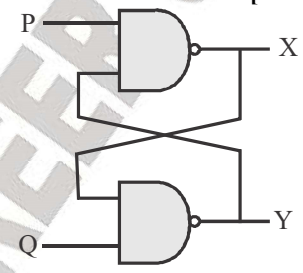


If the input sequence is 10101101001101, starting with the left most bit, then the number of times 'Out' will be 1 is ___

[GATE - 2017]

3. In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is: P = Q = '0', if the input condition is changed simultaneously to P = Q = '1', the outputs X and Y are

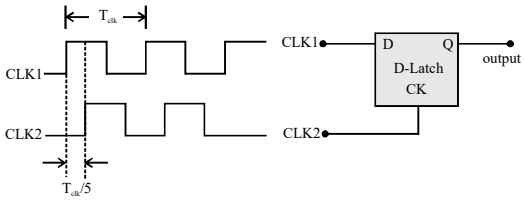
[GATE - 2017]



(a) X = '1', Y = '1'
(b) Either X = '1', Y = '0' or X = '0', Y = '1'
(c) Either X = '1' , Y = '1' or X = '0', Y = '0'
(d) X = '0', Y = '0'

4. Consider the D-latch shown in the figure, which is transparent when its clock input CK is high and has zero propagation delay. In the figure, the clock signal CLK1 has a 50% duty cycle and CLK2 is a one-fifth period delayed version of CLK1. The duty cycle at the output of the latch in percentage is _____.

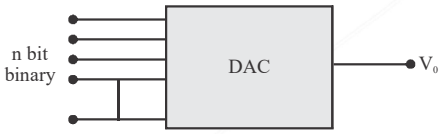
[GATE - 2017]



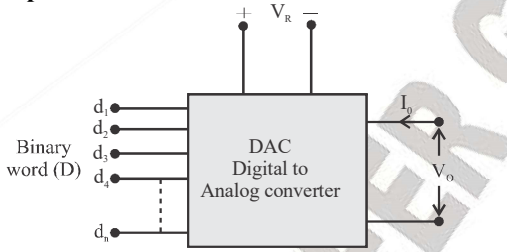
CHAPTER - 5
DIGITAL TO ANALOG CONVERTOR

5.1 DIGITAL TO ANALOG CONVERSION

1. It requires insulation of digital information to an equation analog information.
2. Usually refers as coding device.



Digital to analog convertor specification



5.1.1 Types of DAC

1. Weighted resister DAC
2. R-2R Ladder DAC

5.1.2 Parameter

1. Resolution
2. Analog output voltage
3. V_{Fs}
4. % resolution
5. Error / accuracy

5.1.3 General Equation

$$V_0 = k\{V_{Fs}\left(d_1 2^{-1} + d_2 2^{-2} + ... + d_n 2^{-n}\right)$$

Where, V_{FS} is full scale output voltage k is scaling factor usually "1".

d_1 is MSB with weight of $V_{Fs}/2$

d_n is LSB with weight of $V_{Fs}/2^n$

1. Resolution (D to A converter)

(i)Resolution of DAC is change in analog voltage corresponding to 1 bit LSB increment.

Step size = $\text{Resolution} = \frac{v_r}{2^n - 1}$

Where n is number of bit

v_r is reference voltage corresponding to logic 1.

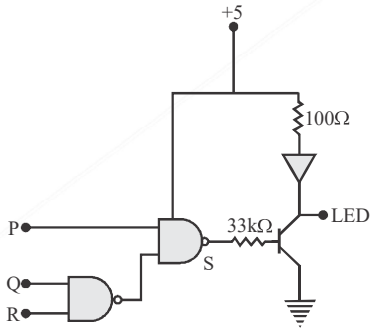
(ii) It is smallest change in analog output.

ASSIGNMENT

1. An 8 bit SAR ADC has full scale reading of 2.55V and its conversion time for an analog input of 1V is 20μs. Conversion time for a 2V input will be

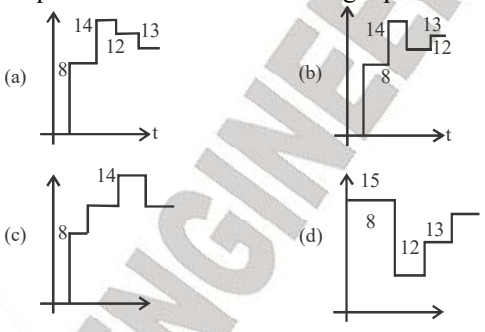
(a) 10μs (b) 50 μs
(c) 40 μs (d) 20μs

2. The logic expression for S′ for the LED in the following circuit to glow in terms of P, Q and R



(a) PQ + QR + PR (b) PQR
(c) $\overline{P}+QR$ (d) P + Q + R

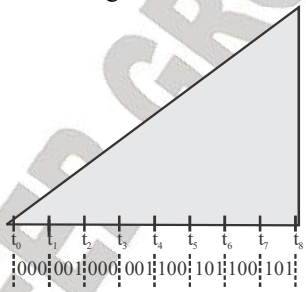
3. Consider a 4-bit successive approximation Register output is fed to DAC. Whose step size is 1V. The full scale output of DAC is + 15V. Which of the following waveforms indicate the output of DAC. When the analog input is 13V.



4. The resolution of an n-bit DAC with max input of 5V is 5mV. The value of n is

(a) 10 (b) 8
(c) 5 (d) 9

5. The input to a 3 bit ADC is as follows and the output code assigned is as drawn



What is the observation about the ADC?
(a) The ADC is perfect
(b) The ADC is not having a stucked 0 LSB
(c) The ADC is having a stucked 0 LSB
(d) The ADC is having a stucked '0' middle bit

6. An 8 bit digit ramp ADC with 40 mV resolution and a clock of 2.5 MHz. When a 6V is applied to the ADC input, what will be the value of output?

(a) 10010111 (b) 10010110
(c) 10111101 (d) 10111111

7. In a 4 bit binary weighted-resistor DAC, the resistor value corresponding to MSB is 2kΩ. The resistor value corresponding to LSB is

(a) 2k/16Ω (b) 2k ×8Ω
(c) 2k/4Ω (d) 2k × 4Ω

8. In a dual slope integrating ADC, the first integration is carried out for 10 periods of the supply frequency of 50 Hz. If the reference voltage used is 2V, the total conversion time for an input of IV is,

(a) 0.5 Sec (b) 0.1 Sec
(c) 0.2 Sec (d) 0.3 Sec

CHAPTER - 6
DIGITAL LOGIC FAMILIES

6.1 INTRODUCTION

1.Basically there are two types of semiconductor devices such as bipolar, unipolar, and based on these devices; integrated circuit (digital) have been made which are commercially available.

2.Various digital functions are being fabricated in a variety of form by using bipolar and unipolar technologies.

3.A group of (compatible IC's) with the same logic level and supply voltage for performing various logic families have been fabricated using a specific circuit configuration which is referred as logic family.

4.The various parameter or characteristics of digital IC's used to compare their performances are:

(i)Speed of operation
(ii)Power dissipation
(iii)Figure of Merit
(iv)Fan out
(v)Current/voltage parameter
(vi)Noise Immunity
(vii)Operating Temperature Range
(viii)Power supply Requirement
(ix)Flexibilities Available

6.2 THERE ARE TWO TYPES OF LOGIC FAMILIES

1.Bipolar Logic Family

(i) Saturated
(a) RTL(Resistor Transistor Logic)
(b) DCTL
(c) I^2L
(d) DTL
(e) TTL
(f) HTL

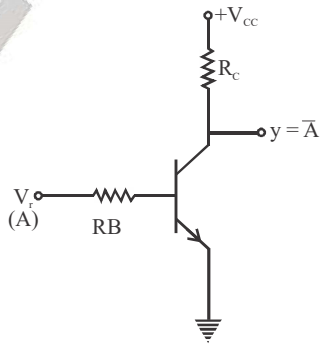
(ii)Unsaturated/Non-saturated
(a) Schottky TTL
(b) ECL(Emitter Coupled Logic)

2. Unipolar Logic Family

(i) MOS: MOSFET are employed in MOS Logic
(a)NMOS
(b)PMOS
(c)CMOS(Complementary Metal Oxide Semiconductor)
(d)BiCMOS uses CMOS for input and logic operation and Bipolar Devices for output.

6.3 BASIC CONCEPTS OF LOGIC FAMILIES ANALYSES

Basic switching element:



SOLUTIONS

Sol 1. (a)

Sol 2. (a)

Sol 3. (a)

Sol 4. (c)

Sol 5. (c)

Sol 6. (c)
ECL circuits are non saturated logic circuits where transistors always operated under active and cutoff region. Hence it is the fastest logic among all the logic circuits.

Sol 7. (c)

Sol 8. (c)

Sol 9. (b)
In I^2L family, p-n-p and n-p-n transistors are integrated together dur to this transistors will occupy less space hence density is more than any other logic family.

Sol 10. (c)
Figure of merit = $P_{disc} \times t_{pd}$ = mW × ns = Pj

Sol 11. (c)

Sol 12. (c)

Sol 13. (a)
Figure of merit = (Propagation delay time) × (power dissipation)

Sol 14. (a)
Fan out of CMOS is high.

Sol 15. (c)
Trisate logic gates have three possible output states i.e., the logic '1' state, the logic '0' state and high-impedance state.

Sol 16. (a)
ECL gate has faster speed (2 ns propagation delay) of operation, than TTL (10 ns) and others. In ECL, the transistor are never in saturation, the input/output voltages have a small swing, the input impedance is high and output resistance is low, as a result, transistors charge states quickly.

Sol 17. (c)

Sol 18. (b)
CMOS-Lower power consumption.

Sol 19. (a)
I^2L -multiple collectors.

Sol 20. (d)
Totem pole refers to the output buffer.

Sol 21. (a)
Reason is the correct explanation of assertion.

Sol 22. (d)
CMOS has high input impedance and low output impedance.

Sol 23. (b)
It is also known as speed power product.

Sol 24. (c)
A. HTL-High Noise Immunity
B. CMOS-High Fanout
C. I^2L-Lowest product of power and delay
D. ECL-Highest speed of operation.

Sol 25. (d)

Sol 26. (c)

Sol 27. (a)
RTL does not have high switching speed.