GATE 2019

DIGITAL ELECTRONICS

ELECTRICAL ENGINEERING

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CONTENTS

CHAPTER - 1
NUMBER SYSTEM

1.1 DATA REPRESENTATION

Magnitude Representation	Complement Representation
1.Unsigned magnitude representation (positive): No sign bit **2.**Signed magnitude representation (positive, negative): One extra bit (sign) as MSB	**1.** (r–1)'s complement: (positive, negative) **2.** R's complement: (positive, negative) MSB = 0 (positive) MSB = 1 (negative)

1.1.1 Sign Magnitude Representation

"+" sign before a number indicate that it is positive (+ve) number and negative (–ve) sign before a number indicate that it is –ve number.

Replace +ve = 0 (MSB); –ve = 1 (MSB)

Example.

$(+1100101)_2 \rightarrow (01100101)_2$

$(+\ 101.001)_2 \rightarrow (0101.001)_2$

$(-10010)_2 \rightarrow (110010)_2$

$(-110.101)_2 \rightarrow (1110.101)_2$

1.1.2 Signed Representation

Ranges is identical as that of 1's complement is also has 2 unique representation for zero

Range = $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$

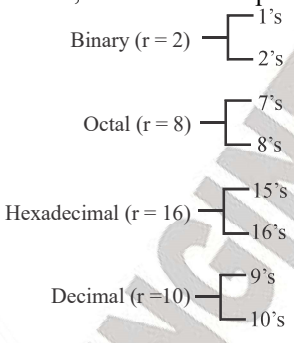
(n = 7): (– 63) to (+ 63)

1.1.3 Complement

There are two type of complements:

1. (r –1)'s complement
2. (r)'s complement

Where, r is base of complement



(r–1)'s complements: To determine the complement subtract the given no form maximum number possible in base.

GATE QUESTIONS

1. The number of bytes required to represent the decimal number 1856357 in packed BCD (Binary Coded Decimal) from is _____.

[GATE - 2014]

2. Which of the following is an invalid state in an 8-4-2-1 Binary coded decimal counter

[GATE - 2014]

(a) 1 0 0 0 (b) 1 0 0 1
(c) 0 0 1 1 (d) 1 1 0 0

3. The two numbers represented in signed 2's complement form are P=11101101 and Q=11100110. If Q is subtracted from P, the value obtained in signed 2's complement form is

[GATE - 2008]

(a) 100000111 (b) 00000111
(c) 11111001 (d) 111111001

4. X=01110 and Y=11001 are two 5-bit binary numbers represent in two's complement format. The sum of X and Y represented in two's complement format using 6 bit is :

[GATE - 2007]

(a) 100111 (b) 001000
(c) 000111 (d) 101001

5. The Octal equivalent of HEX and number AB.CD is

[GATE - 2007]

(a) 253.314 (b) 253.632
(c) 526.314 (d) 526.632

6. A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example the base-5 number 24 will be represented by its BCP code 010100. In the numbering system the BCP code 100010011001 corresponds to the following number in base –5 systems

[GATE - 2006]

(a) 423 (b) 1324
(c) 2201 (d) 4231

7. Decimal 43 in Hexadecimal and BCD number system is respectively

[GATE - 2005]

(a) B2, 0100 0011 (b) 2B, 0100 0011
(c) 2B, 0011 0100 (d) B2, 0100 0100

8. The range of signed decimal numbers that can be represented by 6-bite 1's complement number is

[GATE - 2004]

(a) –31 to +31 (b) –63 to +64
(c) –64 to +63 (d) –32 to +31

9. 11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number?

[GATE - 2004]

(a) 25, 9 and 57 respectively
(b) –6, –6 and –6 respectively
(c) –7, –7 and –7 respectively
(d) –25, –9 and –57 respectively

10. –bit 2's complement representation of a decimal number is 1000. The number is

[GATE - 2002]

(a) +8 (b) 0
(c) –7 (d) –8

11. The 2's complement representation of –17 is

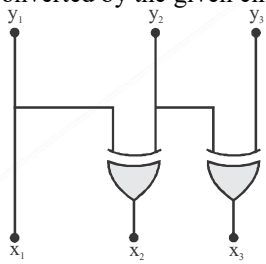
[GATE - 2001]

(a) 01110 (b) 01111
(c) 11110 (d) 10001

ASSIGNMENT

1. When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero?
(a) Sign magnitude
(b) 1's complement
(c) 2's complement
(d) 9's complement

2. In the following codes a binary number $Y_1Y_2Y_3$ is converted by the given circuit.



(a) Excess-3 Code (b) Gray Code
(c) Decimal Code (d) BCD Code

3. Addition of all the gray code to convert decimal (0-9) into gray code is:
(a) 129 (b) 108
(c) 69 (d) 53

4. Input

(a) + 255 (b) +127
(b) +31 (d) Zero

5. If $(123)_5 = (X3)_Y$, then the number of possible values of X is
(a) 4 (b) 3
(c) 2 (d) 1

6. A computer has the following negative numbers stored in binary form as shown. The wrongly stored number is:
(a) –37 as 11011011
(b) –89 as 10100111
(c) –48 as 11101000
(d) –32 as 11100000

7. Octal equivalent of hexadecimal AFAFAF is
(a) 53276757 (b) 76727673
(c) 53727657 (d) 76727672

8. $(177)_8 + 1 = (X)_8$, the value of x is
(a) 178 (b) 179
(c) 200 (d) None of these

9. Noting that $3^2=9$, formulate a simple procedure for converting base–3 numbers directly to base –9 use the procedure to convert $(2110201102220112)_3$ to base 9.
(a) $(66582614)_9$
(b) $(2206112414)_9$
(c) $(73642815)_9$
(d) None of these

10. Identify the first 10 decimal digits in Base 4 number system
(a) 0, 1, 2, 3, 4, 5, 6, 0, 1, 2
(b) 0, 1, 2, 3, 4, 5, 6, 7, 0, 1
(c) 0, 1, 2, 3, 10, 11, 12, 13, 14
(d) 0, 1, 2, 3, 10, 11, 12, 13, 20, 21

11. What is the 11's complement of $(935)_{12}$?
(a) 124_{11} (b) 234_{10}
(c) 286_{12} (d) 330_{10}

12. X and Y are successive digits in a positional number system. Also $XY = 25_{10}$ and $YX = 31_{10}$. Determine the Radix value of the system and value of X and Y.
(a) 6, 4, 2 (b) 7, 3, 4
(c) 7, 4, 3 (d) 6, 4, 3

13. Consider the signed Binary numbers A = 01000110 and B = 11010011, where B is in 2's complement from. Match the following.

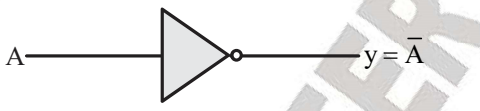
List-I	List-II

CHAPTER - 2
LOGIC GATES & BOOLEAN ALGEBRA

2.1 LOGIC GATE

1.The fundamental building block of digital system. Logic gate means that output and input pattern of gate are assigned logically.
2.The inter connection of Gate to perform a variety of logical operation is called logic design.
3.The input and output of logic gate can occur only in two levels. These level are termed as high (1) and Low (0) simply.
4.Truth table show how the logic circuit o/p respond to various combination of logic level of i/p.
There are various types of gates:
(i)Basic Gates: NOT, AND & OR
(ii)Universal Gate: NAND & NOR
(iii)EXOR & ENOR: Arithmetic, comparator, code converter, parity generator and parity checker.

1. NOT Gate



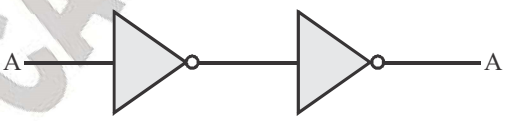
Truth Table

A	y
0	1
1	0

(i)

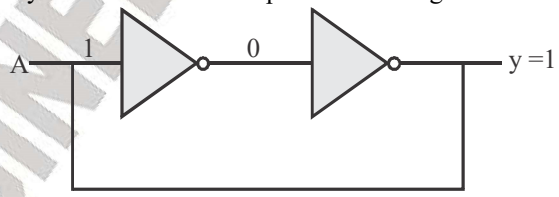
Switching Diagram

(ii)



Buffer Storage

(iii) It act as basic memory element or cross coupled latch storage element

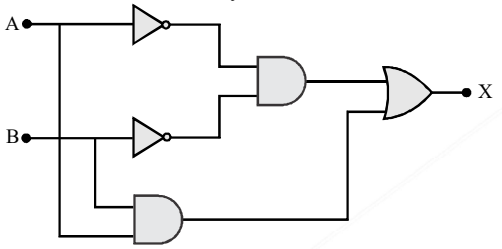


Basic Memory Element

Or mostly represented as

GATE QUESTIONS

1. A and B are the logical inputs and X is the logical output shown in the figure. The output X is related to A and B by



[GATE - 2017]

(a) $X = \overline{A}B + \overline{B}A$ (b) $X = AB + \overline{B}A$

(c) $X = AB + \overline{A}\,\overline{B}$ (d) $X = \overline{A}\,\overline{B} + \overline{B}A$

2. Figure 1 shows a 4-bit ripple carry adder realized using full adders and figure 2 shows the circuit of a full adder (FA). The propagation delay of the XOR, AND and OR gates in figure 2 are 20ns, 15ns and 10 ns, respectively. Assume all the inputs to the 4-bit adder are initially reset to 0.

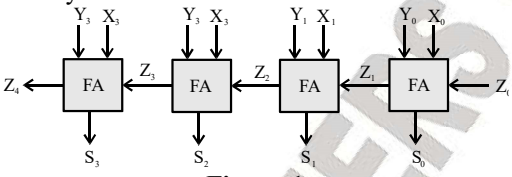


Figure-1

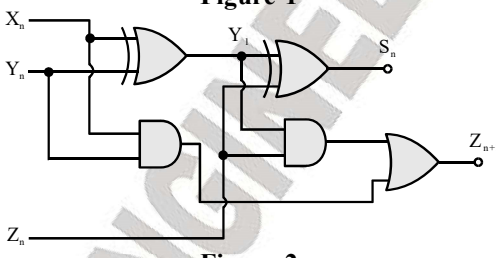
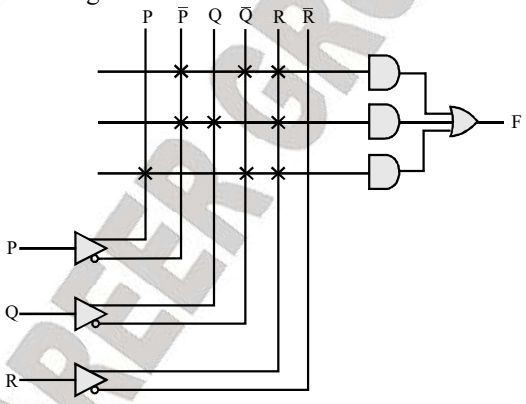


Figure-2

At t = 0, the inputs to the 4-bit adder are changed to $X_3X_2X_1X_0$ = 1100, $Y_3Y_2Y_1Y_0$ = 0100 and Z_0 = 1. The output of the ripple carry adder will be stable at t (in ns) = _____

[GATE - 2017]

3. A programmable logic array (PLA) is shown in the figure.



The Boolean function F implemented is

[GATE - 2017]

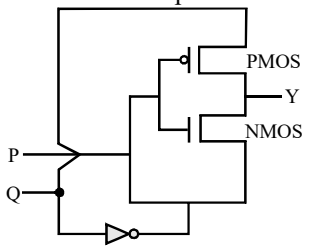
(a) $\overline{P}\,\overline{Q}R + \overline{P}QR + P\overline{Q}\,\overline{R}$

(b) $(\overline{P}+\overline{Q}+R)(\overline{P}+Q+R+(P+\overline{Q}+\overline{R})$

(c) $\overline{P}\,\overline{Q}R + \overline{P}QR + P\overline{Q}\,\overline{R}$

(d) $(\overline{P}+\overline{Q}+R)(\overline{P}+Q+R)+(P+\overline{Q}+\overline{R})$

4. For the circuit shown in figure, P and Q are the inputs and Y is the output.



The logic implemented by the circuit is

[GATE - 2017]

CHAPTER - 3
COMBINATIONAL IC'S

3.1 INTRODUCTION

1.Gates are available as SSI′s.
2.Adder, Multiplexer, Comparators and Encoder's are available in MSI.
3.SSI gates are mainly used for realizing simple Logic functions normally encountered in inter-counting.

3.1.1 Sequential logic

Logic circuits whose output are determined by the sequence in which input signals are applied

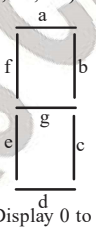
3.1.2 Glitch

A momentry (short pulse) Duration pulse.
For any logic Design it is always essential to design a product which meets the requirement as:
1. Minimum cost
2. Minimum space requirement
3. Maximum speed of operation
4. Easy availability of component
5. Ease of inter connection of component
6. Easy to Design

Example.

Basic Tool used in combinational circuit analysis is Karnaugh map (k-Map)
If we design this display by 4 bit then form (0 to 9) = BCD code valid and A to F (all status are invalid)

$$f(A,B,C,D) = \sum(0,1,2,3....9) + d\sum(10,11,12,13,14)$$



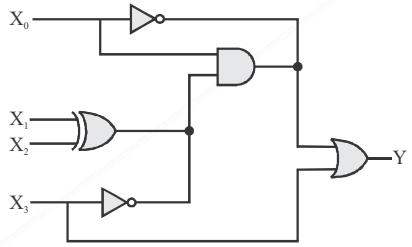
Display 0 to 9

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	x	x	x	x
10	1	1	x	x

$$f(A,B,C,D) = \bar{B} + \bar{C}\bar{D} + CD$$

GATE QUESTIONS

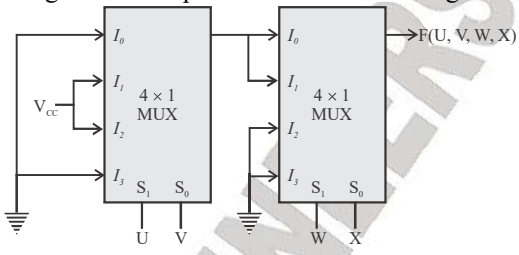
1. The logic gates shown in the digital circuit below use strong pull-down nMOS transistors for LOW logic level at the outputs. When the pull-downs are off, high-value resistors set the output logic levels to HIGH (i.e. the pull-ups are weak). Note that some nodes are intentionally shorted to implement "wired logic". Such shorted nodes will be HIGH only if the outputs of all the gates whose outputs are shorted are HIGH.



The number of distinct values $X_3\ X_2\ X_1\ X_0$ (out of the 16 possible values) that give Y = 1 is _____.

[GATE - 2018]

2. A four-variable Boolean function is realized using 4 × 1 multiplexes as shown in the figure.



The minimized expression for F(Uttar Pradesh V, W, X) is

[GATE - 2018]

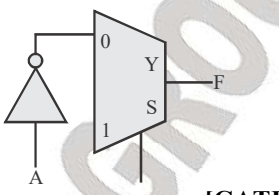
(a) $(UV+\bar{U}\bar{V})\bar{W}$

(b) $(UV+\bar{U}\bar{V})(\bar{W}\bar{X}+\bar{W}X)$

(c) $(U\bar{V}+\bar{U}V)\bar{W}$

(d) $(U\bar{V}+\bar{U}V)(\bar{W}\bar{X}+\bar{W}X)$

3. Consider the following circuit which uses a 2-to-1 multiplexer as shown in the figure below. The Boolean expression for output F in terms of A and B is

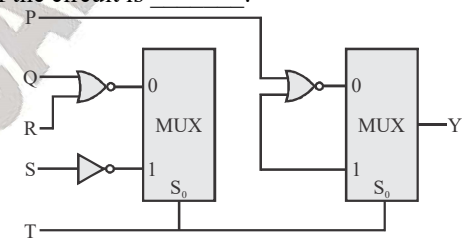


[GATE - 2016]

(a) A⊕B (b) $\overline{A+B}$

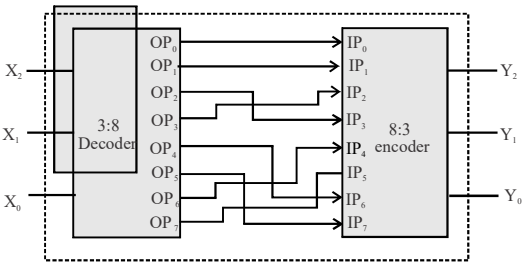
(c) A+B (d) $\overline{A \oplus B}$

4. For the circuit shown in figure, the delays of NOR gates, multiplexer and inverters are 2ns, 1.5ns and 1ns, respectively. If all the inputs P,Q,R,S and T are applied at the same time instant, the maximum propagation delay (in ns) of the circuit is _____.



[GATE - 2016]

5. Identify the circuit below

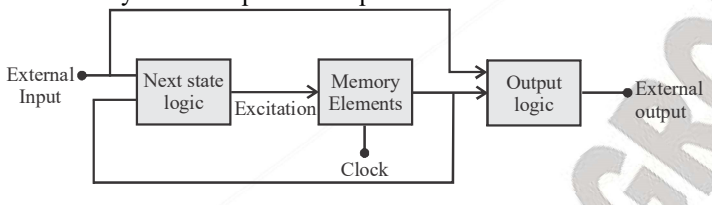


[GATE - 2016]

CHAPTER - 4
SEQUENTIAL LOGIC ANALYSIS

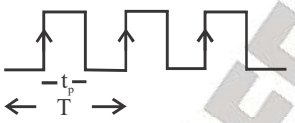
4.1 INTRODUCTION

In combinational circuit the present o/p depend only upon the present input any prior level. (Input condition) does not have any effect on present output.



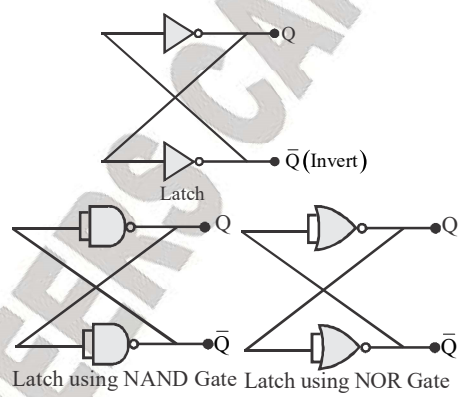
Next state depends upon next state logic and clock is used to receive & store data.

Timing Diagram



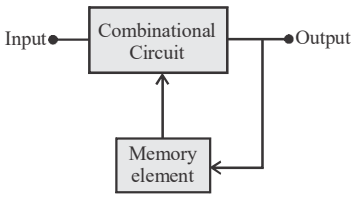
Where $t_p << T$

4.1.1 Bit Memory Cell



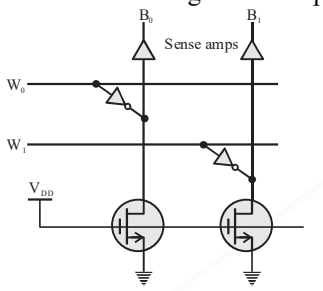
Bistable (MV) Latch Element (1 Bit memory device)

Block Diagram



GATE QUESTIONS

1. A 2 × 2 ROM array is built with the help of diodes as shown in the circuit below. Here W_0 and W_1 are signals that select the word lines and B_0 and B_1 are signals that are output of the sense amps based on the stored data corresponding to the bit lines during the read operation.



$$\begin{array}{c} \\ W_0 \\ W_1 \end{array}\begin{array}{c} \begin{array}{cc} B_0 & B_1 \end{array} \\ \begin{bmatrix} D_{00} & D_{01} \\ D_{10} & D_{11} \end{bmatrix} \end{array}$$

Bits stored in the ROM Array

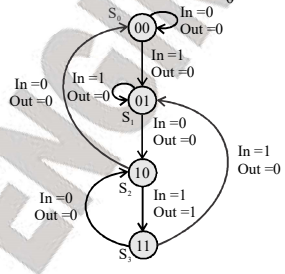
During the read operation, the selected word line goes high and the other word line is in a high impedance state. As per the implementation shown in the circuit diagram above, what are the bits corresponding to D_{ij} (where I = 0 or 1 and j = 0 or 1) stored in the ROM?

[GATE - 2018]

(a) $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$ (b) $\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$

(c) $\begin{bmatrix} 1 & 0 \\ 1 & 0 \end{bmatrix}$ (d) $\begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix}$

2. The state diagram of a finite state machine (FSM) designed to detect an overlapping sequence of three bits is shown in the figure. The FSM has an input 'In' and an output 'out'. The initial state of the FSM is S_0.

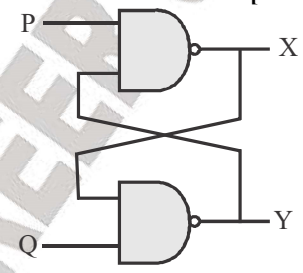


If the input sequence is 10101101001101, starting with the left most bit, then the number of times 'Out' will be 1 is ___

[GATE - 2017]

3. In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is: P = Q = '0', if the input condition is changed simultaneously to P = Q = '1', the outputs X and Y are

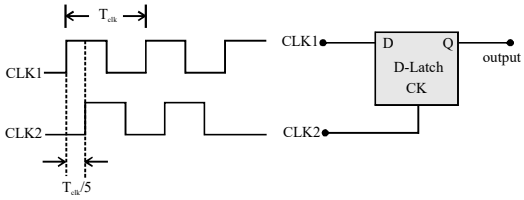
[GATE - 2017]



(a) X = '1', Y = '1'
(b) Either X = '1', Y = '0' or X = '0', Y = '1'
(c) Either X = '1' , Y = '1' or X = '0', Y = '0'
(d) X = '0', Y = '0'

4. Consider the D-latch shown in the figure, which is transparent when its clock input CK is high and has zero propagation delay. In the figure, the clock signal CLK1 has a 50% duty cycle and CLK2 is a one-fifth period delayed version of CLK1. The duty cycle at the output of the latch in percentage is _____.

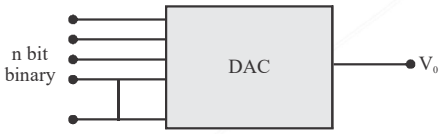
[GATE - 2017]



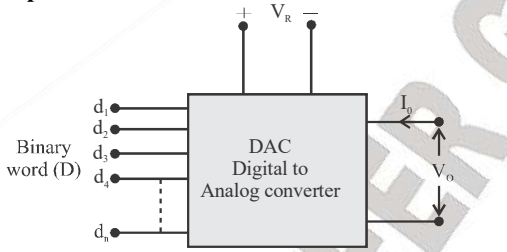
CHAPTER - 5
DIGITAL TO ANALOG CONVERTOR

5.1 DIGITAL TO ANALOG CONVERSION

1. It requires insulation of digital information to an equation analog information.
2. Usually refers as coding device.



Digital to analog convertor specification



5.1.1 Types of DAC

1. Weighted resister DAC
2. R-2R Ladder DAC

5.1.2 Parameter

1. Resolution
2. Analog output voltage
3. V_{Fs}
4. % resolution
5. Error / accuracy

5.1.3 General Equation

$$V_0 = k\{V_{Fs}\left(d_1 2^{-1} + d_2 2^{-2} + ... + d_n 2^{-n}\right)$$

Where, V_{FS} is full scale output voltage k is scaling factor usually "1".

d_1 is MSB with weight of $V_{Fs}/2$

d_n is LSB with weight of $V_{Fs}/2^n$

1. Resolution (D to A converter)

(i)Resolution of DAC is change in analog voltage corresponding to 1 bit LSB increment.

Step size = $\text{Resolution} = \frac{v_r}{2^n - 1}$

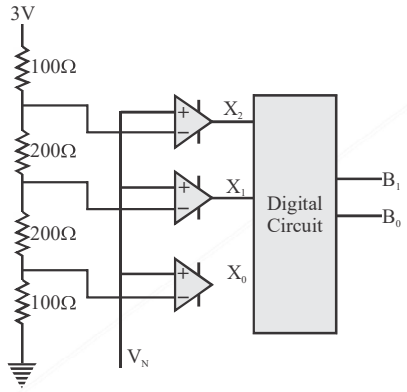
Where n is number of bit

v_r is reference voltage corresponding to logic 1.

(ii) It is smallest change in analog output.

GATE QUESTIONS

1. A 2-bit flash Analog to Digital Converter (ADC) is given below. The input is $0 \le V_N \le 3$ Volts. The expression for the LSB of the output B_0 as a Boolean function of X_2, X_1 and X_0 is

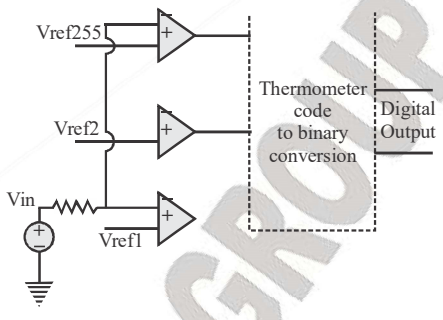


[GATE - 2016]

(a) $X_0[\overline{X_2 \oplus X_1}]$ (b) $\overline{X}_0[\overline{X_2 \oplus X_1}]$

(c) $X_0[X_2 \oplus X_1]$ (d) $\overline{X}_0[X_2 \oplus X_1]$

2. In an N bit flash ADC, the analog voltage is fed simultaneously to $2^N - 1$ comparators. The output of the comparators is then encoded to a binary format using digital circuit. Assume that the analog voltage source Vin (whose output is being converted to digital format) has a source resistance of 75Ω as shown in the circuit diagram below and the input capacitance of each comparator is 8pF. The input must settle to an accuracy of ½ LSB even for a full scale input change for proper conversion. Assume that the time taken by the thermometer to binary encoder is negligible.



If the flash ADC has 8 bit resolution, which one of the following alternatives is closest to the maximum sampling rate?

[GATE - 2016]

(a) 1 mega samples per second
(b) 6 mega samples per second
(c) 64 mega samples per second
(d) 256 mega samples per second

3. Consider a four bit D to A convener. The analog value corresponding to digital signals of values 0000 and 0001 are 0 V and 0.0625 V respectively. The analog value (in Volts) corresponding to the digital signal 1111 is____

[GATE - 2015]

4. Consider a four bit D to A convener the analog value corresponding to digital signals of values 0000 and 0001 are 0 V and 0.0625 V respectively. The analog value (in Volts) corresponding to the digital signal 1111 is _____.

[GATE - 2015]

5. If WL is the Word Line and BL the Bit Line, an SRAM cell is shown in

CHAPTER - 6
DIGITAL LOGIC FAMILIES

6.1 INTRODUCTION

1.Basically there are two types of semiconductor devices such as bipolar, unipolar, and based on these devices; integrated circuit (digital) have been made which are commercially available.

2.Various digital functions are being fabricated in a variety of form by using bipolar and unipolar technologies.

3.A group of (compatible IC's) with the same logic level and supply voltage for performing various logic families have been fabricated using a specific circuit configuration which is referred as logic family.

4.The various parameter or characteristics of digital IC's used to compare their performances are:

(i)Speed of operation
(ii)Power dissipation
(iii)Figure of Merit
(iv)Fan out
(v)Current/voltage parameter
(vi)Noise Immunity
(vii)Operating Temperature Range
(viii)Power supply Requirement
(ix)Flexibilities Available

6.2 THERE ARE TWO TYPES OF LOGIC FAMILIES

1.Bipolar Logic Family

(i) Saturated
(a) RTL(Resistor Transistor Logic)
(b) DCTL
(c) I^2L
(d) DTL
(e) TTL
(f) HTL

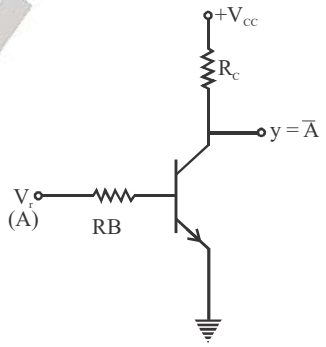
(ii)Unsaturated/Non-saturated
(a) Schottky TTL
(b) ECL(Emitter Coupled Logic)

2. Unipolar Logic Family

(i) MOS: MOSFET are employed in MOS Logic
(a)NMOS
(b)PMOS
(c)CMOS(Complementary Metal Oxide Semiconductor)
(d)BiCMOS uses CMOS for input and logic operation and Bipolar Devices for output.

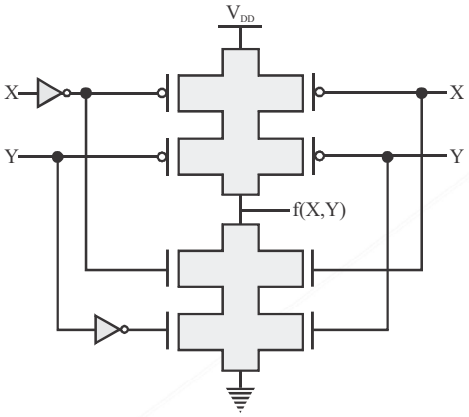
6.3 BASIC CONCEPTS OF LOGIC FAMILIES ANALYSES

Basic switching element:



GATE QUESTIONS

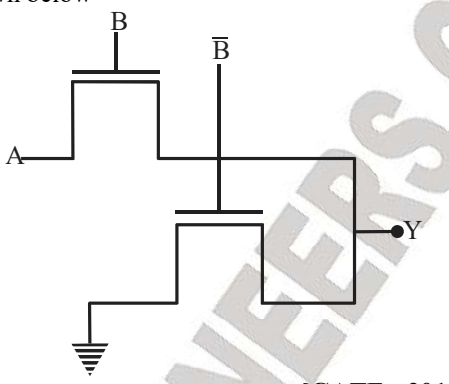
1. The logic f(X, Y) realized by the given circuit is



[GATE - 2018]

(a) NOR (b) AND
(c) NAND (d) XOR

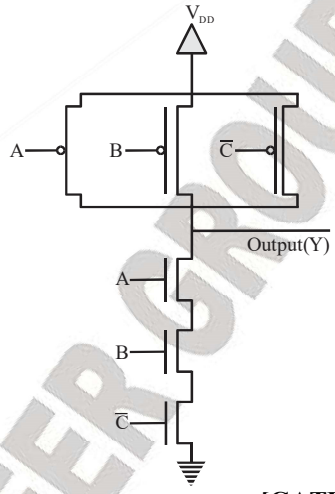
2. The logic functionality realized by the circuit shown below is



[GATE - 2016]

(a) OR (b) XOR
(c) NAND (d) AND

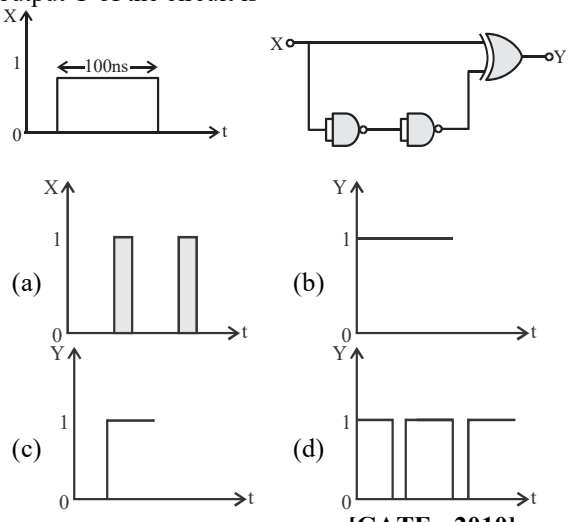
3. The output (Y) of the circuit shown in the figure is



[GATE - 2014]

(a) $\overline{A}+\overline{B}+C$ (b) $A+\overline{B}\cdot\overline{C}+A\cdot\overline{C}$
(c) $\overline{A}+B+\overline{C}$ (d) $A\cdot B\cdot\overline{C}$

4. The TTL circuit shown in the figure is fed with the waveform X (also shown). All gates have equal propagation delay of 10 ns. The output Y of the circuit is



[GATE - 2010]

ASSIGNMENT

1. Which has least power dissipation
(a) TTL (b) Schottky TTL
(c) CEL (d) CMOS

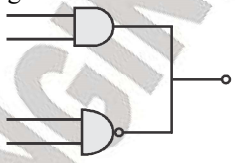
2. The TTL open collector output of two 2-input NAND gates are connected to a common pull-up resistor. If the inputs of the gates are A, B, C and D are respectively. The output is equal to
(a) $\overline{A \cdot B} \cdot \overline{C \cdot D}$ (b) $\overline{A \cdot B} + \overline{C \cdot D}$
(c) $A \cdot B + C \cdot D$ (d) $A \cdot B \cdot C \cdot D$

3. A three input NAND gates is used to be as an inverter. Which of the following measures will achieve better results?
(a)The two inputs not used are kept open
(b)The two inputs not used are connected to ground (0 level)
(c)The two inputs not used are (connected to supply V_{DD} (1 level)
(d)None of the above

4. For I_{OL}(max) = 16mA, I_{IL}(max) = 0.0016A, find out
(a) 16 (b) 10
(c) 1.6 (d) 100

5. The basic gate of ECL family is,
(a) NAND (b) NOR
(c) XOR (d) AND

6. Which one of the following logic functions is implemented by the gates when their open collector type outputs are tied together as shown in the given figure?



(a) $F = AB + C + D$ (b) $F = \overline{AB(C + D)}$
(c) F = AB + (C + D) (d) $F = \overline{AB + C + D}$

7. In which of the following option, the logic families are arranged in the decreasing order of Power dissipation?
(a) TTL, DTL, CMOS
(b) CMOS, TTL, DTL
(c) TTL, CMOS, DTL
(d) DTL, CMOS, TTL

8. In a standard TTL, totem pole refers to
(a) Multi emitter stage
(b) The phase splitter
(c) CMOS, TTL, DTL
(d) DTL, CMOS, TTL

9. In a standard TTL, totem pole refers to
(a) Multi emitter stage
(b) The phase splitter
(c) The output buffer
(d) Open collector output stage

10. In TTL floating input to a gate is considered
(a) Logical 0
(b) Logical 1
(c) Either 0 or 1
(d) Gate O/P will be undefined

11. The figure of merit of a logic is given by
(a)Gain bandwidth product
(b)Propagation delay and power dissipation product
(c)Fan out and propagation delay product
(d)Noise margin and power dissipation product

12. Match list-I with list-II and select the correct answer using the code given below in the list

List-I	**List-II**
A. HTL	(i)High fan out
B. CMOS	(ii)Highest speed of operation
C. I^2L	(iii)High noise immunity
D. ECL	(iv)Lowest product of power and delay

Codes: