GATE 2019

DIGITAL LOGIC

COMPUTER SCIENCE

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Website: www.engineerscareergroup.in **Toll Free:** 1800-270-4242

E-Mail: ecgpublica ons@gmail.com | info@engineerscareergroup.in

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CHAPTER - 1
NUMBER SYSTEM

1.1 DATA REPRESENTATION

Data can be any digit, character or any symbol. And it can be represented in following categories.

Magnitude Representation	Complement Representation
1. Unsigned magnitude representation (positive): No sign bit **2.** Signed magnitude representation (positive, negative): One extra bit (sign) as MSB	**1.** (r–1)'s complement: (positive, negative) **2.** r's complement: (positive, negative) MSB = 0 (positive) MSB = 1 (negative)

1.1.1 Sign Magnitude Representation

1. "+" sign before a number indicates that it is positive (+ve) number and negative (–ve) sign before a number indicates that it is –ve number. Replace +ve with MSB 0 and –ve with MSB 1 followed by binary equivalent of given number to get its sign representation.

2. Range is identical as that of 1's complement and also has 2 unique representation for zero. Its Range = $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$ such as for n = 7 range is (– 63) to (+ 63)

Example

$(+1100101)_2 \rightarrow (01100101)_2$
$(+\ 101.001)_2 \rightarrow (0101.001)_2$
$(-10010)_2 \rightarrow (110010)_2$
$(-110.101)_2 \rightarrow (1110.101)_2$

1.1.2 Complement

There are two types of complements:

1. (r – 1)'s complement

2. (r)'s complement , Where , r = base of complement

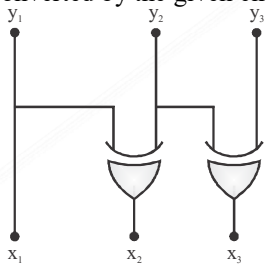
- Binary (r = 2)
  - 1's complement
  - 2's complement
- Octal (r = 8)
  - 7's complement
  - 8's complement
- Hexadecimal (r = 16)
  - 15's complement
  - 16's complement
- Decimal (r =10)
  - 9's complement
  - 10's complement

(r–1)'s Complement: To determine this complement, subtract the given number from maximum number having number of digits equal to the number of digits in given number possible in given base.

ASSIGNMENT

1. When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero?
(a) sign magnitude (b) 1's complement
(c) 2's complement (d) 9's complement

2. In the following codes a binary number $Y_1Y_2Y_3$ is converted by the given circuit



(a) Excess-3 Code (b) Gray Code
(c) Decimal Code (d) BCD Code

3. Addition of all the gray codes to convert decimal (0-9) into gray code is:
(a) 129 (b) 108
(c) 69 (d) 53

4. Input

(a) + 255 (b) +127
(b) +31 (d) Zero

5. If $(123)_5 = (x3)_y$, then the number of possible values of x is
(a) 4 (b) 3
(c) 2 (d) 1

6. A computer has the following negative numbers stored in binary form as shown. The wrongly stored number is:
(a) –37 as 11011011
(b) –89 as 10100111
(c) –48 as 11101000
(d) –32 as 11100000

7. Octal equivalent of hexadecimal AFAFAF is
(a) 53276757 (b) 76727673
(c) 53727657 (d) 76727672

8. $(177)_8 + 1 = (X)_8$, the value of x is
(a) 178 (b) 179
(c) 200 (d) None of these

9. Noting that $3^2 = 9$, formulate a simple procedure for converting base – 3 numbers directly to base – 9 use the procedure to convert $(2110201102220112)_3$ to base 9.
(a) $(66582614)_9$
(b) $(2206112414)_9$
(c) $(73642815)_9$
(d) None of these

10. Identify the first 10 decimal digits in Base 4 number system
(a) 0, 1, 2, 3, 4, 5, 6, 0, 1, 2
(b) 0, 1, 2, 3, 4, 5, 6, 7, 0, 1
(c) 0, 1, 2, 3, 10, 11, 12, 13, 14
(d) 0, 1, 2, 3, 10, 11, 12, 13, 20, 21

11. What is the 11's complement of $(935)_{12}$?
(a) 124_{11} (b) 234_{10}
(c) 286_{12} (d) 330_{10}

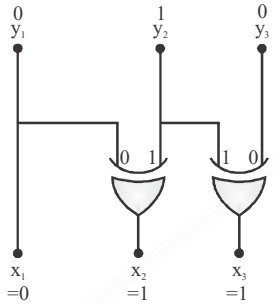
12. X and Y are successive digits in a positional number system. Also $XY = 25_{10}$ and $YX = 31_{10}$. Determine the Radix value of the system and value of X and Y.
(a) 6, 4, 2 (b) 7, 3, 4
(c) 7, 4, 3 (d) 6, 4, 3

13. Consider the signed Binary numbers A = 01000110 and B = 11010011, where B is in 2's complement form. Match the following.
List-I
A. A + B
B. A – B
C. B – A
D. A – B
List-II

SOLUTIONS

Sol. 1 (c)

Sol. 2 (c)



Let us take the binary input 010

∴ It forms a gray code.

Binary Code	Gray Code
000	000
001	001
010	011
011	010
100	110
101	111
110	101
111	100

Sol. 3 (d)

Decimal	BCD	Gray Code	Decimal Equivalent of Gray
0	0000	0000	0
1	0001	0001	1
2	0010	0011	3
3	0011	0010	2
4	0100	0110	6
5	0101	0111	7
6	0110	0101	5
7	0111	0100	4
8	1000	1100	12
9	1001	1101	13
		Total=	+53

Sol. 4 (b)

$X_1 = 1\ 0\ 1\ 0\ 1\ 0\ 1\ 0$, $X_2 = 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$

$X_1 \oplus X_2$=?

X_1	X_2	$X_1 \oplus X_2$
1	1	0
0	1	1
1	1	0
0	1	1
1	1	0
0	1	1
1	1	0
0	1	1

Binary number: $(0\ 1\ 0\ 1\ 0\ 1\ 0\ 1)_2$

Binary to Gray Code: $(0\ 1\ 1\ 1\ 1\ 1\ 1\ 1)_2$

Gray code to Decimal:

$=0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 1 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$

$=64 + 32 + 16 + 8 + 4 + 2 + 1 = +127$

Sol. 5 (c)

$(123)_5 = (x3)_y$ then

$1\times5^2 + 2 \times 5^1 + 3 \times 5^0 = x.y^1 + 3.y^0$

$25 + 10 + 3 = xy + 3$

$35 = xy$

Possible factor of 35 are:

1×35 : when y = 35, x = 1 is possible.

35× 1: when y = 1, x = 35 is not possible

5× 7 : when y = 7, x = 5 is possible.

7 × 5: when y = 5, x = 7 is not possible.

Hence x has 2 possible values.

Sol. 6 (c)

$48_{10} = 00110000$

11001111

$+\ 1$

$-48_{10} = 11010000$

$37_{10} = 00100101$

$1\quad 11011010$

$+\ 1$

$-37_{10} = 11011011$

GATE QUESTIONS

1. Given the following binary number in 32-bit (single precision) IEEE – 754 format:
00111110011011010000000000000000
The decimal value closest to this floating – point number is

[GATE - 2017]

(a) 1.45×10^{1} (b) 1.45×10^{-1}
(c) 2.27×10^{-1} (d) 2.27×10^{1}

2. The representation of the value of a 16- bit unsigned integer X in hexadecimal number system is BCA9. The representation of the value of X in octal number system is

[GATE - 2017]

(a) 57124 (b) 736251
(c) 571247 (d) 136251

3. Let X be the number of distinct 16-bit integers in 2's complement representation. Let Y be the number of distinct 16-bit integers in sign magnitude representation. Then X–Y is_____.

[GATE - 2016]

4. The 16-bit 2's complement representation of an integer is 1111 1111 1111 0101; its decimal representation is _____.

[GATE - 2016]

5. Consider the equation $(43)_x = (y3)_8$ where x and y are unknown. The number of possible solutions are _____.

[GATE - 2015]

6. The number of bytes required to represent the decimal number 1856357 in packed BCD (Binary Coded Decimal) from is _____.

[GATE - 2014]

7. Which of the following is an invalid state in an 8-4-2-1 Binary coded decimal counter

[GATE - 2014]

(a) 1 0 0 0 (b) 1 0 0 1
(c) 0 0 1 1 (d) 1 1 0 0

8. Consider the equation $(123)_5 = (x8)_y$ with x and y as unknown. The number of possible solutions are _____.

[GATE - 2014]

9. The base (or radix) of the number system such that the following equation $\frac{312}{20} = 13.1$ holds is _____.

[GATE - 2014]

10. The decimal value 0.5 in IEEE single precision floating point representation has

[GATE - 2012]

(a) Fraction bits of 000…000 and exponent value of 0
(b) Fraction bits of 000…000 and exponent value of – 1
(c) Fraction bits of 100…000 and exponent value of 0
(d) No exact representation

11. $(1217)_8$ is equivalent to

[GATE - 2009]

(a) $(1217)_{16}$ (b) $(028F)_{16}$
(c) $(2297)_{10}$ (d) $(0B17)_{16}$

12. The two numbers represented in signed 2's complement form are P=11101101 and Q=11100110. If Q is subtracted from P, the value obtained in signed 2's complement form is

[GATE - 2008]

(a)100000111 (b) 00000111
(c)11111001 (d)111111001

13. In the IEEE floating point representation the hexadecimal value 0x00000000 corresponds to

[GATE - 2008]

(a) The normalized value 2^{-127}
(b) The normalized value 2^{-126}
(c) The normalized value + 0
(d) The special value + 0

CHAPTER - 2
LOGIC GATES & BOOLEAN ALGEBRA

2.1 LOGIC GATE

1. The fundamental building block of digital system Logic gate means that o/p and i/p pattern of gate are assigned logically.

2. The inter connection of Gates is to perform a variety of logical operations is called logic design.

3. The input and output of logic gate can occur only in two levels. These levels are termed as high (1) and Low (0) simply.

4. Truth table show how the logic circuit o/p responds to various combination of logic levels of i/p.

5. There are various types of gates

(i) Basic Gates: NOT, AND & OR

(ii) Universal Gate: NAND & NOR

(iii) EXOR & ENOR: Arithmetic, comparator, code converter, parity generator and parity checker.

2.1.1 Basic Gates

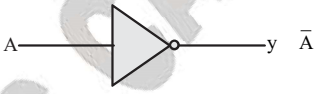
1. NOT Gate

(i) It is one –input and one-output gate.

(ii) Its output is inverted to its corresponding input. If input is 1 then its output is 0 and if its input is 0 then its output is 1.

(iii) It is called inverter.

(iv) It is represented by following symbol

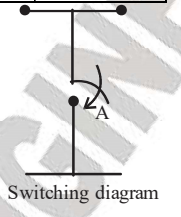


(v) Its all possible input combination and its corresponding output can be represented in the form of table called Truth Table. Truth table for NOT gate is following

Truth Table

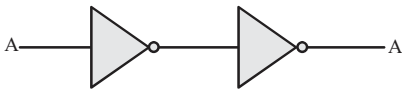
A	y
0	1
1	0

(i)



Switching diagram

(ii)



Buffer Storage

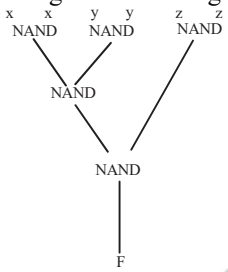
(vi) It act as basic memory element or cross coupled latch storage element and represented as

ASSIGNMENT

1. Which of the following logic expression is incorrect?
(a) $1 \oplus 0 = 1$ (b) $1 \oplus 1 \oplus 0 = 1$
(c) $1 \oplus 1 \oplus 1 = 1$ (d) $1 \oplus 1 = 0$

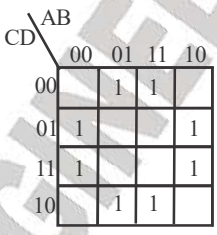
2. Which of the following Boolean algebra statements represent distributive law?
(a) (A+B) +C = A + (B+C)
(b) A. (B+C) = (A.B) + (A.C)
(c) A.(B.C) = (A.B).C
(d) None of these

3. Which expression is computed by the following NAND-gate circuit diagram?



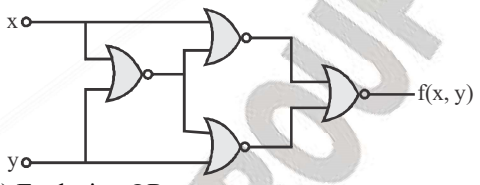
(a) x′y′+z (b) (x+y) z′
(c) x′y′z (d) x′+y′+z′

4. What is the equivalent Boolean expression in product of sum form for the K-map given below?



(a) BD′+B′D
(b) (B+C′+D) (B′+C+D′)
(c) (B+D′) (B′+D)
(d) (B′+D′) (B+D)

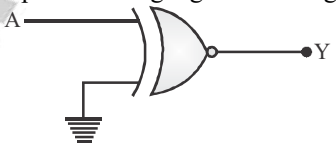
5. Identify the logic function performed by the circuit.



(a) Exclusive OR
(b) Exclusive NOR
(c) NAND
(d) NOR

6. The binary number 110011 is to be converted to gray code. The number of gates and type required are:
(a) 6, AND (b) 6, XNOR
(c) 6, XOR (d) 5, XOR

7. The output of the logic gate in the figure is



(a) AB + AC +BC (b) A +BC
(c) $\overline{A}$ (d) A + B + C

8. What is the minimum number of NAND gates required to implement $A + A\overline{B} + A\overline{B}C$
(a) 0 (b) 1
(c) 4 (d) 7

9. If x and y are Boolean variables, which one of the following is the equivalent of $x \oplus y \oplus xy$.
(a) x+y′ (b) x+y
(c) 0 (d) 1

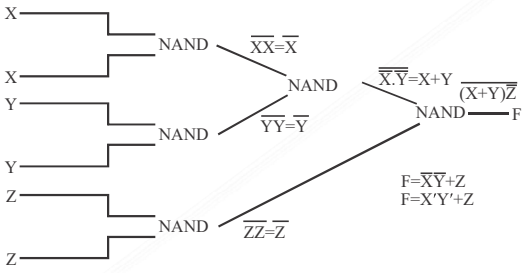
10. Consider the following gate network which of following gates is redundant?

SOLUTIONS

Sol. 1 (b)

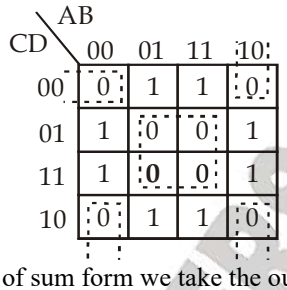
Sol. 2 (a)

Sol. 3 (d)



Hence answer is (a)

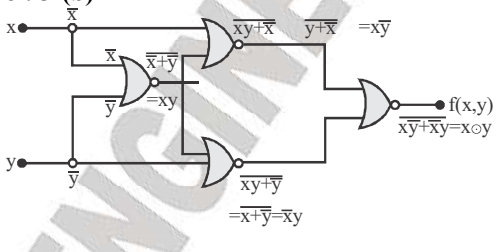
Sol. 4 (d)



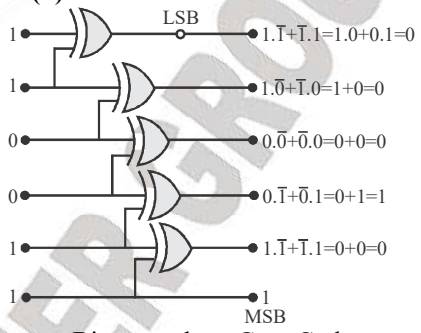
In product of sum form we take the output as 0

$(\overline{B}+\overline{D})(B+D)$

Sol. 5 (b)



Sol. 6 (d)



It converts Binary code to Gray Code.

110011 is converted to 1 0 1 0 1 0

$\therefore$ 5 – XOR gates are required.

Sol. 7 (c)

Ground(G)	A	$G \rightarrow A$
0	0	1
0	1	0

$\therefore$ The Output is complemented.

Sol. 8 (a)

$F = A + A\overline{B} + A\overline{B}C = A + A\overline{B}(1+C)$

$= A + A\overline{B} = A(1+\overline{B})$

$\therefore$ It contains one AND gate and one OR gate, No NAND gate is required.

Sol. 9 (b)

$= x \oplus y \oplus xy = (x\overline{y} + \overline{x}y) \oplus xy$

$= (x\overline{y} + \overline{x}y)\overline{xy} + xy\left[\overline{x\overline{y} + \overline{x}y}\right]$

$= (x\overline{y} + \overline{x}y)(\overline{x} + \overline{y}) + xy\left[xy + \overline{x}\,\overline{y}\right]$

$= x\overline{x}\overline{y} + \overline{x}\,\overline{x}y + x\overline{y}\,\overline{y} + \overline{x}y\overline{y} + (xy.xy) + xy.\overline{x}\,\overline{y}$

$\because \left[A.\overline{A} = 0, A.A = A\right]$

$\therefore\ \overline{x}y + x\overline{y} + xy$

$= \overline{x}y + x(y + \overline{y}) \quad (\because A + \overline{A} = 1)$

(a) $W, Y, XZ, \overline{X}\overline{Z}$ (b) W, Y, XZ

(c) $Y, \overline{X}\overline{Y}\overline{Z}$ (d) $Y, XZ, \overline{X}\overline{Z}$

17. The Boolean expression

$(X+Y)(X+\overline{Y})+(\overline{X\,\overline{Y}})+\overline{X}$ simplifies to

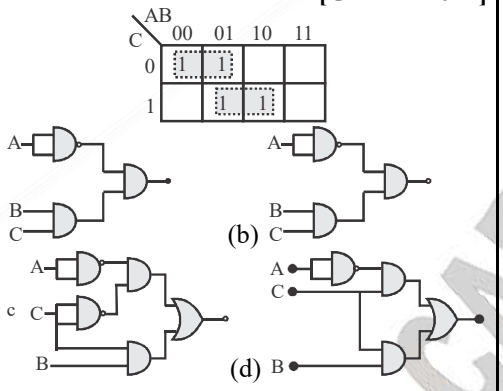
[GATE - 2014]

(a) X (b) Y

(c) XY (d) X+Y

18. Which of the following logic circuits is a realization of the function F whose Karnaugh map is shown in figure.

[GATE - 2014]



19. The SOP (sum of products) form of a Boolean function is $\Sigma(0,1,3,7,11)$, where input are A, B, C, D (A is MSB, and D is LSB). The equivalent minimized expression of the function is

[GATE - 2014]

(a) $(\overline{B}+C)(\overline{A}+C)(\overline{A}+\overline{B})(\overline{C}+D)$

(b) $(\overline{B}+C)(\overline{A}+C)(\overline{A}+\overline{C})(\overline{C}+D)$

(c) $(\overline{B}+C)(\overline{A}+C)(\overline{A}+\overline{C})(\overline{C}+\overline{D})$

(d) $(\overline{B}+C)(A+\overline{B})(\overline{A}+\overline{B})(\overline{C}+D)$

20. Let $\oplus$ denotes the Exclusive OR (XOR) operation. Let '1' and '0' denote the binary constants. Consider the following Boolean expression for F over two variables P and Q.

$F(P, Q) = ((1\oplus P)\oplus(P\oplus Q))\oplus((P\oplus Q)\oplus(Q\oplus 0))$

The equivalent expression for F is

[GATE - 2014]

(a) P + Q (b) $\overline{P+Q}$

(c) $P \oplus Q$ (d) $\overline{P\oplus Q}$

21. Consider the following minterms expression for F:F(P,Q,R,S)=$\sum$(0,2,5,7,8,10,13 ,15) The minterms 2, 7, 8 and 13 are 'do not care' terms. The minimal sum - of - products form for F is

[GATE - 2014]

(a) $Q\overline{S}+\overline{Q}S$

(b) $\overline{Q}\overline{S}+QS$

(c) $\overline{Q}\overline{R}\overline{S}+\overline{Q}R\overline{S}+Q\overline{R}S+QRS$

(d) $\overline{P}\overline{Q}\overline{S}+\overline{P}QS+P\overline{Q}\overline{S}$

22. The dual of a Boolean function $F(x_1, x_2,\ldots x_n,+, \cdot, ')$, written as F^D, is the same expression as that of F with + and · swapped. F is said to be self dual if $F = F^D$. The number of self – dual functions with n Boolean variable is

[GATE - 2014]

(a) 2^n (b) 2^{n-1}

(c) 2^{2^n} (d) $2^{2^{n-1}}$

23. Consider the following Boolean expression for F:

$F(P, Q, R, S) = PQ + \overline{P}QR + \overline{P}Q\overline{R}S$

The minimal sum of products form of F is

[GATE - 2014]

(a) PQ + QR + QS (b) P + Q + R + S

(c) $\overline{P}+\overline{Q}+\overline{R}+\overline{S}$ (d) $\overline{P}R+\overline{P}\overline{R}S+P$

24. Which one of the following expression does NOT represent exclusive NOR of x and y?

[GATE - 2014]

(a) xy + x′y′ (b) $x \oplus y'$

(c) $x' \oplus y$ (d) $x' \oplus y'$

25. In the sum of products function f (X,Y,Z) = $\sum$(2,3,4,5),the prime implications are

[GATE - 2012]

(a) $\overline{X}Y, X\overline{Y}$

(b) $\overline{X}Y, X\overline{Y}\overline{Z}.X\overline{Y}Z$

(c) $\overline{X}Y\overline{Z}, \overline{X}YZ\ XY$

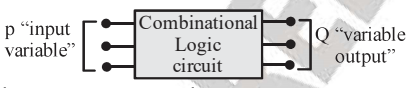
(d) $\overline{X}Y\overline{Z}, \overline{X}YZ, X\overline{Y}\overline{Z}, X\overline{Y}Z$

CHAPTER - 3
COMBINATIONAL LOGIC CIRCUIT

3.1 INTRODUCTION
For any logic Design it is always essential to design a product which meets the requirement as:
1.Minimum cost
2. Minimum space requirement
3. Maximum speed of operations
4. Easy availability of component
5. Ease of inter connection of components
6. Easy to Design

3.1.1 Sequential Logic
Logic circuits whose outputs are determined by the sequence in which input signals are applied.

3.2 COMBINATIONAL CIRCUITS
The circuits whose output depends upon the current input combinations only are called combinational circuits.



Where p is input binary variable term as external source.
And Q is output variable go to external destination.

3.2.1 Design Procedure
1. Statement is assigned with variable analysis.
2. The no. of input and output variable is determined
3. The logic that defined the relation between input and output are determined
4. Logic function diagram is associated

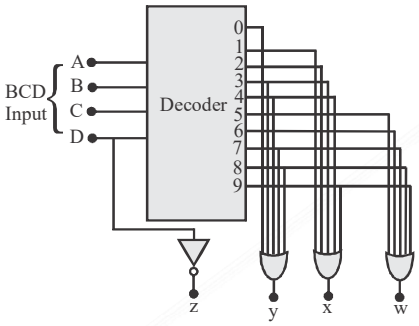
3.2.2 Characteristic of Combinational circuit
1. Present output depends on only the present input
2. No feedback is available/present
3. No storage (many) element is required
Example.
(i) Adder and Subtractor
(ii) Multiplexer and De-Multiplexer
(iii) Decoder and Encoder

3.3 ARITHMETIC COMBINATIONAL CIRCUIT
Adder and Subtractor are Arithmetic combinational circuits.

3.3.1 Half Adder
It adds only any two bits and gives their sum and carry.

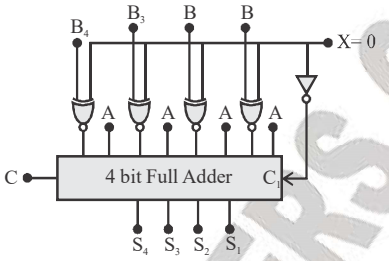
ASSIGNMENT

1. The following logic circuit f(w, x, y, z) indicates



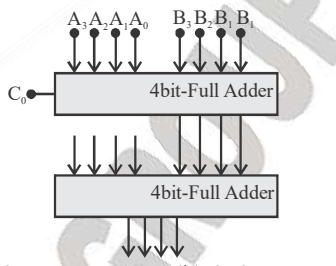
(a) Binary to BCD converter
(b) BCD to Binary converter
(c) BCD to Decimal converter
(d) BCD to Excess – 3 converter

2. Identify the function of the following logic circuit



(a) 4 – bit Binary adder
(b) 4 – bit BCD Adder
(c) 4 – bit Binary subtractor
(d) 4 – bit BCD subtractor

3. The following logic circuit adds two digits represented in the Excess - 3 code. The correction required after adding the two digits in EX-3 form is as follows.
If $C_0 = 1$ and + 3
Identify the inputs to be given to the 2^{nd} 4 - bit full adder?



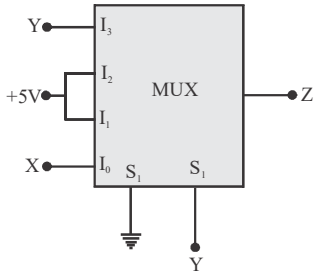
(a) $C_0, C_0, 0, C_0$ (b) $0, 0, C_0, C_0$
(c) $0, 0, C_0, C_0$ (d) $\overline{C}_0, \overline{C}_0, \overline{C}_0, 1$

4. A Boolean function F with A, B, C as inputs is expressed on Karnaugh map as shown below. If this function is implemented with 4 : 1 multiplexer as B, C selection lines, identify the input connections

A \ BC	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$			1	
A	1	1		1

(a) A, A, $\overline{A}$, 1 (b) A, A, 1, $\overline{A}$
(c) A, 1, $\overline{A}$, 0 (d) A, A, $\overline{A}$, A

5. The output of the 4 × 1 multiplexer shown in figure is



(a) $X + Y$ (b) $\overline{X}\overline{Y} + X$
(c) $X\overline{Y}$ (d) $\overline{X} + \overline{Y}$

6. Identify the output of the following logic circuit

SOLUTIONS

Sol. 1 (d)
From truth table of BCD to excess – 3 code
$z = \overline{D}$
$y = \sum m(0,3,4,7,8)$
$x = \sum m(1,2,3,4,9)$
$w = \sum m(5,6,7,8,9)$

Sol. 2 (c)
It is 4 – bit binary subtractor

Sol. 3 (d)
If $C_0 = 1$ and 3 means i/p to 2nd 4 – bit full adder should be 0011 $\Rightarrow \overline{C}_0\overline{C}_0C_0 1$
If $C_0 = 0$ subtract 3 means i/p to 2nd 4 – bit full adder should be 1101 $\Rightarrow \overline{C}_0\overline{C}_0C_0 1$ So i/p to 2nd adder should be $\overline{C}_0\overline{C}_0C_0 1$.

Sol. 4 (d)
From K – map

A \ BC	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	0	0	1	0
A	1	1	0	1

When BC = 00, o/p is equal to A, so $I_0 = A$
When BC = 01, o/p is equal to A, so $I_1 = A$
When BC = 10, o/p is equal to A, so $I_2 = A$

Sol. 5 (a)
$Z = Y + \overline{Y}X$
$= (Y + \overline{Y})(X + Y) = X + Y$

Sol. 6 (a)
$F = \overline{X}_1\overline{X}_2 + X_1X_2 = X_1 \odot X_2$

Sol. 7 (d)
For full adder Sum = A ⊕ B ⊕ C and
Carry = AB + C (A ⊕ B)
So it requires 2 2 input X-OR , 2 input AND 1,2 2 input OR gates.

Sol. 8 (c)
For Sum = 20 + 20 = 40ns
For Carry = 20 + 10 + 10 = 40ns

Sol. 9 (b)
$X = [(A \oplus B)C] + [(AB) \oplus C]$
$= (A\overline{B} + \overline{A}B)C + AB\overline{C} + \overline{AB}C$
$= A\overline{B}C + \overline{A}BC + AB\overline{C} + \overline{A}C + \overline{B}C$

Sol. 10 (c)
$X = \overline{A}C + \overline{B}C + B\overline{C}$
So there are 5 literal $\overline{A}, \overline{B}, C, B$ and $\overline{C}$

Sol. 11 (c)
O/P of AND gate is (x y) $(x\overline{y}) = 0$
$F = D_0 + D_1 = \overline{O}\overline{A}_0 + \overline{O}A_0 = \overline{O} = 1$

Sol. 12 (c)
Output of first MUX $= \overline{b}\overline{a} + ab = a \odot b$
$Z_1 = \overline{c}\overline{(a \odot b)} + (a \odot b)c$
$= a \odot b \odot c$
$Z_2 = \overline{(a \odot b)}b + (a \odot b)c$
$= (a\overline{b} + \overline{a}b)b + (ab + \overline{a}\overline{b})c$
$= \overline{a}b + abc + \overline{a}\overline{b}c$
$= \overline{a}b + bc + \overline{a}c$

Sol. 13 (b)
$Y = \overline{A}0 + AB = AB$

Sol. 14 (d)
To construct a 5 × 32 line decoder 11 1-to-4 decoders are used.

Sol. 15 (a)
For C_5 generation, 4 carry generation path will come into path.

Sol. 16 (c)
Total delay = 31 × 12 + 42 = 414 ns

Sol. 17 (c)

GATE QUESTIONS

1. When two 8-bit numbers A_7 ….. A_0 and B_7 ….B_0 in 2's complement representation (with A_0 and B_0 as the least significant bits) are added using a ripple - carry adder, the sum bits obtained are S_7….. S_0 and the carry bits are C_7…… C_0 . an overflow is said to have occurred if

[GATE - 2017]

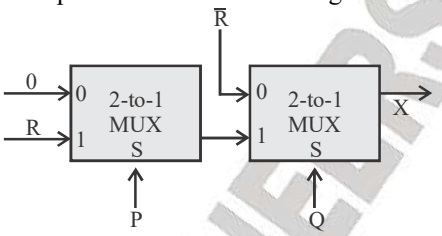
(a) The carry bit C_7 is 1
(b) All the carry bits (C_7 , …… , C_0) are 1
(c) $(A_7.B_7.\overline{S}_7 + \overline{A}_7.-\overline{B}_7.S_7)$ is 1
(d) $(A_0.B_0.\overline{S}_0 + \overline{A}_0.-\overline{B}_0.S_0)$ is 1

2. Consider a carry look ahead adder for adding two n-bit integers, built using gates of fan-in at most two. The time to perform addition using this adder is

[GATE - 2016]

(a) Θ(1) (b) Θ(log(n))
(c) Θ(n) (d) Θ(n)

3. Consider the two cascaded 2-to-1 multiplexers as shown in the figure.



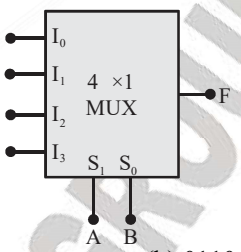
The minimal sum of products form of the output X is

[GATE - 2016]

(a) P Q + P′Q′R (b) PQ+QR
(c) PQ′ + P′QR (d) Q′R′ + PQR

4. In the 4 × 1 multiplexer, the output F is given by F = A ⊕ B. Find the required input '$I_3I_2I_1I_0$'.

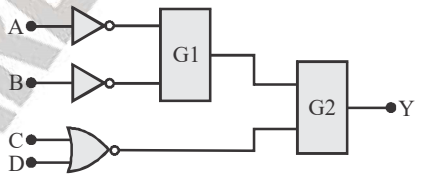
[GATE - 2015]



(a) 1010 (b) 0110
(c) 1000 (d) 1110

5. In the figure shown, the output Y is required to be $Y = AB + \overline{C}\,\overline{D}$. The gates G1 and G2 must be, respectively

[GATE - 2015]



(a) NOR, OR (b) OR, NAND
(c) NAND, OR (d) AND, NAND

6. A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using full adders. The total propagation time of this 4-bit binary adder in microseconds is _____.

[GATE - 2015]

7. The number of min-terms after minimizing the following Boolean expression is _____
[D′ + AB′ + A′C + AC′D + A′C′D]′

[GATE - 2015]

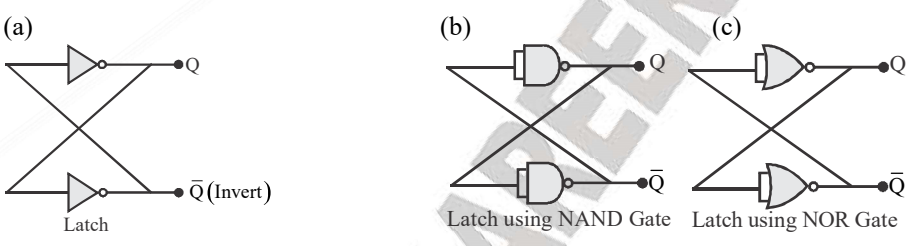
CHAPTER - 4
SEQUENTIAL LOGIC CIRCUIT

4.1 INTRODUCTION

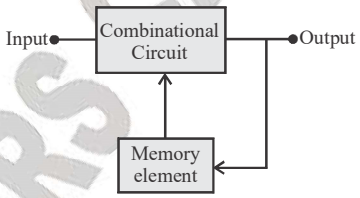
1. In combinational circuit the present O/P depends only upon the present input any prior level. (Input condition) does not have any effect on present output.
2. In sequential circuits, Present output depends upon the present input combinations as well as previous outputs of the system. Therefore, sequential circuits have feedback property.

4.2 1-BIT MEMORY CELL

1. The following circuits are designed to store 1-bit data. They use feedback property hence they are sequential circuits that are the simplest.**2.** Information stored in memory element at any given time define the present state of sequential circuit.

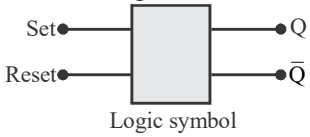


Block Diagram



4.3 LATCHES

1. It refers to unclocked flip flop because these flip flop latch on to a "1" or a "0" Imperially upon running the input called "SET" and "RESET".
2. They are not dependent upon the clock signal for their operation.
3. A latch is a sequential device that checks all its inputs continuously and changes its output accordingly at any time independent of clock signals.



4.3.1 S-R Latch using NOR Gate

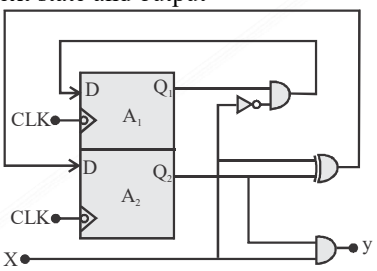
The Set – Reset Latch can be designed using NOR Gates as following

ASSIGNMENT

1. A counter constructed using T – FFs counts the decimal digits according to 2, 4, 2, 1 code. The input T_B is

(a) A′ B + CD (b) A′ B + BCD
(c) A′ B + D (d) A′ B + A′ D

2. A sequential circuit is as shown below. If present states of A_1, A_2, are 1, 0 and x = 1, what is its next state and output

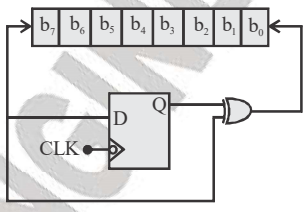


(a) 0, 1, 0 (b) 1, 0, 0
(c) 0, 1, 1 (d) 1, 1, 1

3. In a 4 bit modulo – 6 ripple counter the proportional delay of J-K Flip flop is 50ns. What is the max clock frequency that can used without skipping a count ?

(a) 2MHz (b) 4 MHz
(c) 5 KHz (d) 5 MHz

4. In the following logic circuit, the 8 bit left shift register and D – Flip flop is synchronized with same clock. The D – Flip flop is initially cleared. The circuit acts as



(a) Binary to 2′s complement converter
(b) Binary to EX – 3 code converter
(c) Binary to 1′s complement converter
(d) Binary to Gray code converter

5. A N – bit register is constructed using D – flip – flops. Match the following List-I with List-II

List-I

A. Parallel in parallel out
B. Serial in serial out
C. Parallel in serial out
D. Serial in parallel out

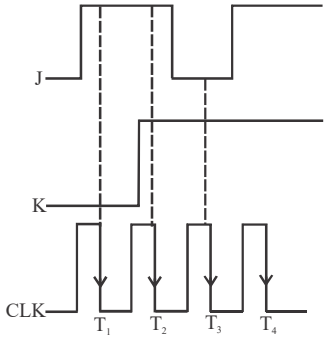
List-II

(i) (2N – 1) clock pulses
(ii) One clock pulses
(iii) N clock pulses
(iv) (N – 1) clock pulses

Codes:

(a) A-iii, B-iv, C-ii, D-i
(b) A-iv, B- ii, C-i, D-iii
(c) A-iii, B-ii, C-iv, D-i
(d) A-ii, B-i, C-iv, D-iii

6. Determine the output of the negative Edge triggered J-K flip flop for the following input waveforms at T_1, T_2, T_3, T_4. Assume the hold time FF is 0.



(a) 0, 1, 0, 1 (b) 0, 1, 1, 0
(c) 1, 0, 0, 1 (d) 1, 0, 1, 1

7. Two J – K FFS having negative edge triggering are connected as shown in figure. Which of the following conditions have to be satisfied for proper functioning of the circuit .

SOLUTIONS

Sol. 1 (a)

Decimal	Present State $Q_AQ_BQ_CQ_D$	Next State $Q_A^+Q_B^+Q_C^+Q_D^+$	$T_AT_BT_CT_D$
0	0 0 0 0	0 0 0 1	0 0 0 1
1	0 0 0 1	0 0 1 0	0 0 1 1
2	0 0 1 0	0 0 1 1	0 0 0 1
3	0 0 1 1	0 1 0 0	0 1 1 1
4	0 1 0 0	1 0 1 1	0 1 1 1
5	1 0 1 1	1 1 0 0	0 1 0 1
6	1 1 0 0	1 1 0 1	0 0 0 1
7	1 1 0 1	1 1 1 1	0 0 1 1
8	1 1 1 0	1 1 1 0	0 0 0 1
9	1 1 1 1	1 1 1 1	1 1 1 1

T_B

AB \ CD	00	01	11	10
00	0	1	1	1
01	1	×	×	×
11	0	0	1	0
10	×	×	1	×

Sol. 2 (c)
Input to A_1 D F/F = 0
Input to A_2 D F/F = 1
so after clock o/p of A_1 and A_2 will be 0, 1 respectively so y = 1.

Sol. 3 (d)
Total propagation delay = 4 × 50 ns
maximum frequency used

$$= \frac{1}{200 \times 10^{-9}} = 5 \times 10^6 \text{ Hz}$$

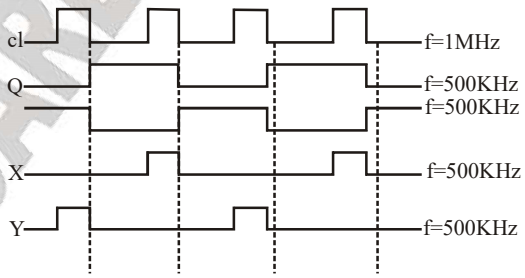
Sol. 4 (d)
Circuit act as binary to gray code convertor

Sol. 5 (d)
Parallel In Parallel out – one clock pulse
Serial in Serial out – (2N – 1) clock pulses
Parallel in serial out – (N – 1) clock pulses
Serial in parallel out – N clock pulses

Sol. 6 (b)
For T_1, J = 1 and K = 0, so Q = 1
For T_2, J = 1 and K = 0, so Q = 0
For T_3, J = 0 and K = 1, so Q = 0
For T_4, J = 1 and K = 1, so Q = 1

Sol. 7 (c)
For proper functioning $t_h < t_{PLH}$, so that 2nd FF can latch proper data.

Sol. 8 (d)
X = Q clock and Y = $\overline{Q}$ clock
So waveforms are as follows



Sol. 9 (c)
Using 3FF counter can count 2^3 = 8 states Therefore, mod – 6 counter will slip 2 counts if it is made of 3FF.

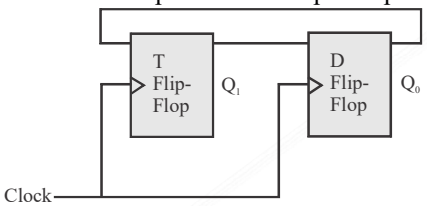
Sol. 10 (d)
When X = $\overline{B}$ and Y = $\overline{C}$, the outputs are cleared at the sequence CBA = 110. For all other states, the counter works in normal operation.

Sol. 11 (a)
For m FF total no. of outcomes (outputs) will be 2m and total number of inputs = n (given). Hence in state table total columns will be total o/p's + total no. of i/p's = 2m +n

Sol. 12 (d)

GATE QUESTIONS

1. Consider a combination of T and D flip – flops connected as shown below. The output of the D flip – flop is connected to the input of the T flip – flop and the output of the T flip – flop is connected to the input of the D flip – flop.



Initially, both Q_0 and Q_1 are set to 1 (before the 1st clock cycle). The outputs

[GATE - 2017]

(a) Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 00 respectively
(b) Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 00 respectively
(c) Q_1Q_0 after the 3rd cycle are 00 and after the 4th cycle are 11 respectively
(d) Q_1Q_0 after the 3rd cycle are 01 and after the 4th cycle are 01 respectively

2. The next state table of a 2-bit saturating up – counter is given below.

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using T flip – flops. The expression for T_1 and T_0 are

[GATE - 2017]

(a) $T_1 = Q_1Q_0, T_0 = \overline{Q_1}\,\overline{Q_0}$
(b) $T_1 = \overline{Q_1}Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$
(c) $T_1 = Q_1 + Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$
(d) $T_1 = \overline{Q_1}Q_0, T_0 = Q_1 + Q_0$

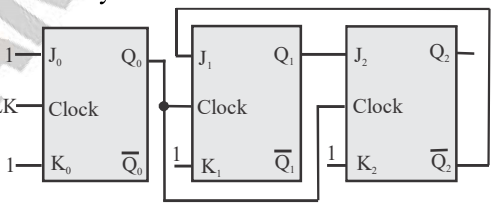
3. We want to design a synchronous counter that counts the sequence 0-1-0-2-0-3 and then repeats. The minimum number of J-K flip-flops required to implement this counter is _____.

[GATE - 2016]

4. Consider an eight-bit ripple-carry adder for computing the sum of A and B, where A and B are integers represented in 2's complement form. If the decimal value of A is one, the decimal value of B that leads to the longest latency for the sum to stabilize is_____.

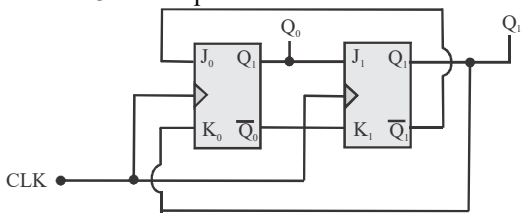
[GATE - 2016]

5. The figure shows a digital circuit constructed using negative edge triggered J – K flip flops. Assume a starting state of $Q_2Q_1Q_0 = 000$. This state $Q_2Q_1Q_0 = 000$ will repeat after _____ number of cycles'.



[GATE - 2015]

6. In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is $Q_1Q_0 = 00$. The state (Q_1Q_0), immediately after the 3rd clock pulse is



[GATE - 2015]

(a) 00 (b) 01
(c) 10 (d) 11

7. The figure shows a binary counter with synchronous clear input. With the decoding logic shown, the counter works as a

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SECTION- A
OPERATING SYSTEM

CHAPTER - 1
BASIC CONCEPTS

1.1 OPERATING SYSTEM

An operating system is a program that manages the computer hardware. It also provides a basis for application programs and acts as an intermediary between the computer user and the computer hardware. The main function of these systems is to dynamically allocate programs. As such, research in this area is clearly concerned with management and scheduling of memory, process and other devices.

1.2 OBJECTIVES OF OPERATING SYSTEM

As operating system are the programs that interface the machine with application programs. It can be having three objectives:

1. Convenience

When we talk about small network or isolated system, an O.S makes a computer more convenient to use.

2. Efficiency

As networking is growing exponentially and if we talk about large scale network then OS allows system resources to be used in an efficient manner.

Dual mode of operation provides the means for protecting the operating system from errant users and errant users from one another.

1.3 FUNCTIONS OF OPERATING SYSTEMS

1. Process Management
2. Memory Management
3. Storage Management
4. Mass-Storage Management
5. Input-Output Systems
6. Protection and Security

1.3.1 Process Management

The operating system is responsible for the following activities in connection with the process management:

1. Scheduling processes and threads on the CPUs
2. Creating and deleting both user and system processes
3. Suspending and resuming processes
4. Providing mechanisms for process synchronization
5. Providing mechanisms for process communication

1.3.2 Memory Management

The operating system is responsible for the following activities in connection with memory management:

1. Keeping track of which parts of memory are currently being used and by whom
2. Deciding which processes (or parts thereof) and data to move into and out of memory
3. Allocating and de-allocating memory space as needed

ASSIGNMENT

Common Data for Q.1 & Q. 2
Consider the following 5 processes with the length of CPU burst time given in milliseconds together with their respective priority.

Process	Burst time	Arrival time
P_1	10	4
P_2	9	1
P_3	1	3
P_4	4	2
P_5	3	2

1. What will be average waiting time in case of priority scheduling?
(a) 10 (b) 11
(c) 12 (d) 13

2. What will be average waiting time in case of FCFS?
(a) 14.6 (b) 15
(c) 16 (d) 17

3. Which will b e average waiting time of R-R scheduling with time quantum of 10?
(a) 15.6 (b) 16.6
(c) 14.6 (d) 15

4. Which of the following statements is/are true?
(a)A batch system is good for running large jobs that do not need interaction
(b)A time sharing system provide illusion of a dedicated interactive system to more than one user.
(c)The real time system must guarantee response to events within fixed periods of time to ensure correct performance
(d)All of these

5. In case of multiprogramming, which of the following is false?
I. The response time is shorter.
II. Throughput is increased
III. Priority can be assigned to jobs
IV. Operating system overhead is decreased
(a) I & II (b) IV only
(c) III & IV (d) I & IV

6. In multiprogramming which of the following is true?
(a) Processor utilization is increased
(b) More than one process can be executed
(c) Response time of a process is shortened
(d) All of these

7. In fork () system call the return value to the parent process and to the child process are respectively,
(a) PID of child process, 1
(b) PID of child process, 0
(c) PID of child process, PID of parent process
(d) 1, PID of parent process

8. Which of the following may block running process?
(a) Fork (b) Read
(c) Down (d) All of these

9. During creation of a user or kernel level thread which of the following is-held by a small data structure?
(i) Register set (ii) stack (iii) priority
(a) Only (i) and (ii) (b) Only (ii) and (iii)
(c) Only (i) and (iii) (d) All

10. Which of the following policy is most suitable in the time-sharing environment?
(a) SJF (b) Round Robin
(c) FCFS (d) SRTF

11. Which of the following best described the term multitasking?
(a)A user can have more than one application open and in use at the same time
(b)Processing time is managed by the operating system so that system resources are optimized

GATE QUESTIONS

1. Which combination of the following features will suffice to characterize an OS as a multi-programmed OS?

[GATE - 2002]

(i) More than one program may be loaded into main memory at the same time for execution.
(ii) If a program waits for certain events such as I/O, another program is immediately scheduled for execution
(iii)If the execution of a program terminates, another program is immediately scheduled for execution
(a) (i) (b) (i) and (ii)
(c) (i) and (iii) (d) (i), (ii) and (iii)

2. A CPU has two modes-privileged and non-privileged. In order to change the mode from privileged to non-privileged

[GATE - 2001]

(a) A hardware interrupt is needed
(b) A software interrupt is needed
(c) A privileged instruction (which does not generate an interrupt) is needed
(d) A non-privileged instruction (which does not generate an interrupt) is needed)

SOLUTIONS

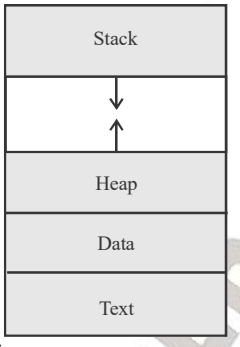
Sol. 1. (d)
(i)Virtual memory helps to load more than one program.
(ii)Multi programming, wait for an I/O of one process can execute other process.
(iii)After completion of one process, other process executes, immediately.

Sol. 2. (d)
For switching between privileged to non-privileged area, non-privileged instruction is used, without interrupt.

CHAPTER - 2
PROCESS MANAGEMENT

2.1 PROCESS

1. Informally, a process is a program in execution. A process includes more than just program code such as current activities, process stock, data section, heap (memory that is dynamically allocated during process runtime).



2. Other definition of process can be given as:
(i) An instance of a program running on a computer.
(ii) The entity that can be assigned to and executed on processor.

2.1.1 Process State

The state of a process is defined by the current activity of that process.
As process executes, it changes its state from one to another state.

2.1.2 Different States of the Process

1.New: The process is being created.
2.Running: Instructions are being executed.
3.Waiting: The process is waiting for some event to occur (such as an I/O completion or reception of a signal)
4.Ready: The process is waiting to be assigned to a processor.
5.Terminated: The process has finished execution.

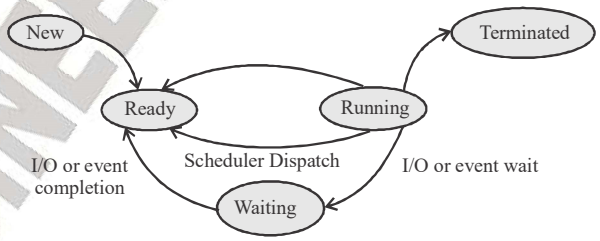


Figure Diagram of process State

2.1.3 Process Control Block

Each process is represented in the operating system a process control block (PCB)
It contains many pieces of information associated with specific process, including these:

ASSIGNMENT-I

1. A thread is usually defined as a 'light weight process' because an Operating System (OS) maintains smaller data structures for a thread than for a process. In relation to this, which of the following is true?
(a)On per-thread basis, the OS maintains only CPU register state
(b)The OS does not maintain a separate stack for each thread
(c)On per-thread basis, the OS does not maintain virtual memory state
(d)On per-thread basis, the OS maintains only scheduling and accounting information\

2. Using priority scheduling algorithm, find the average waiting time for the following set of processes given with their priorities in the order, Process, Burst Time, Priority, respectively as
P_1 : 10 : 3
P_2 : 1 : 1
P_3 : 1 : 1
P_4 : 1 : 5
P_5 : 5 : 2
(a) 8 ms (b) 8.2 ms
(c) 7.75 ms (d) 3 ms

3. Consider the following set of processes, with the length of the CPU burst given in millisecond

Process	Burst time	Priority
P_1	10	3
P_2	1	1
P_3	2	3
P_4	1	4
P_5	5	2

The processes are assumed to have arrived in the order P_1, P_2, P_3, P_4, P_5 all at time 0.
What is the average waiting time of processes in priority scheduling?
(a) 8.2 (b) 8.4
(c) 8.1 (d) 6.2

4. A major problem with priority scheduling is
(a) Definite blocking (b) Starvation
(c) Low priority (d) None of these

5. Consider three processes (process id 0, 1,2, respectively) with compute time bursts 2, 4, and 8 time units. All processes arrive at time zero. Consider the longest remaining time process with the lowest process id. In LRTF ties are broken by giving priority to the process with the lowest process id. The average turnaround time is
(a) 13 units (b) 14 units
(c) 15 units (d) 16 units

6. Assume that the following jobs are to be executed on a single processor system.

Job ID	CPU Burst time
p	4
q	1
r	8
s	1
t	2

The jobs are assumed to have arrived at time 0^+ and in the order p, q, r, s, t. calculate the departure time (completion time) for job p if scheduling is round robin with time slice 1.
(a) 4 (b) 10
(c) 11 (d) 12

7. Pre-emptive scheduling is the strategy of temporarily suspending a running process
(a) Before the CPU time slice expires
(b) To allow starving process to run
(c) When it request I/O.
(d) None of the above

8. Which of the following is an example of a spooled device?
(a)The terminal used to the input data for a program being executed.
(b)The secondary memory device in a virtual memory system.
(c)A line printer used to print the output of a number of jobs
(d)None of the above

GATE QUESTIONS

1. Consider the set of processes with arrival time (in milliseconds). CPU burst time (in milliseconds), and priority (0 is the highest priority) shown below. None of the processes have I/O burst time.

Process	Arrival Time	Burst Time	Priority
P_1	0	11	2
P_2	5	28	0
P_3	12	2	3
P_4	2	10	1
P_5	9	16	4

The average waiting time (in milliseconds) of all the processes using preemptive priority scheduling algorithm is _____.

[GATE - 2017]

2. A system shares 9 taype drives. The current allocation and maximum requirement of tape drives for three processes are shown below:

Process	Current Allocation	Maximum Requirement
P1	3	7
P2	1	6
P3	3	5

Which of the following best describes current state of the system?

[GATE - 2017]

(a) Safe, Deadlocked
(b) Safe, Not Deadlocked
(c) Not Safe, Deadlocked
(d) Not Safe, Deadlocked

3. Recall that Belady's anomaly is that the page–fault rate may increase as the number of allocated frames increases. Now, consider the following statements:
S1: Random page replacement algorithm (where a page chosen at random is replaced) suffers from Belady's anomaly.
S2: LRU page replacement algorithm suffers from Belady's anomaly
Which of the following is CORRECT?

[GATE - 2017]

(a) S1 is true, S2 is true
(b) S1 is true, S2 is false
(c) S1 is false, S2 is true
(d) S1 is false, S2 is false

4. Consider the following CPU processes with arrival times (in milliseconds) and length of CPU bursts (in milliseconds) as given below:

Process	Arrival Time	Burst Time
P1	0	7
P2	3	3
P3	5	5
P4	6	2

If the pre-emptive shortest remaining time first scheduling algorithm is used to schedule the processes, then the average waiting time across all processes is _____ milliseconds.

[GATE - 2017]

5. Consider an arbitrary set of CPU-bound processes with unequal CPU burst lengths submitted at the same time to a computer system. Which one of the following process scheduling algorithms would minimize the average waiting time in the ready queue?

[GATE - 2016]

(a) Shortest remaining time first
(b) Round-robin with time quantum less than the shortest CPU burst
(c) Uniform random
(d) Highest priority first with priority proportional to CPU burst length

6. Consider the following processes, with the arrival time and the length of the CPU burst given in milliseconds. The scheduling algorithm used is preemptive shortest remaining-time first.

CHAPTER - 3
SYNCHRONIZATION

3.1 SYNCHRONIZATION

It means coordinating all concurrent processes accessing the shared data or resources of the system. The process who runs independently are known as "Independent Process" . The process who have dependency on each other are called as "Cooperative Processes". These processes may be shares message, files or logical address space.

3.2 CRITICAL SECTION

It is a segment of code in which the process may be changing common variables, updating shared table, writing a file etc.

No two processes are executing in their critical sections at the same time.

3.2.1 Critical-Section Problem

It is to design a code, which the processes can use to cooperate. General structure of a typical process P_i consists of entry section, Exit Section, Remainder Section.

1. Entry section

It is the section of code implementing the request to enter in the critical section.

2. Exit section

It is the section of code, which allows other processes to enter in the critical section.

3. Remainder section

It is the remaining section of code excluding entry and exit section of the process.

General structure of a typical process to enter in critical section

```
Do
{
    Entry Section
Critical Section
    Exit Section

  While (True);
}
```

The solution to the critical section problem should satisfy the below three criteria's:

(i) Mutual Exclusion

Whenever a process P_i is running in a critical section and any other process who shares this critical section should not be allowed to enter into critical section.

ASSIGNMENT

1. Process P_1 and P_2 have a producer – consumer relationships, communicating by the use of a set of shared buffers:

P_1: repeat obtain an empty buffer Fill it return a full buffer forever	P_2: repeat obtain a full buffer empty it return an empty buffer for ever

Increasing the number of buffers is likely to do which of the following?
1. Increase the rate at which request is satisfied.
2. Decrease the likelihood of deadlock
3. Increase the case of achieving a correct implementation.

(a) 1 only (b) 2 only
(c) 2 and 3 only (d) 1, 2 and 3

2. Consider a queue between the two processes indicated below. N is the length of queue and e,f and b are semaphore.
init: e : = N; f : = 0 b : = 1

Process : 1	Process : 2
loop p(e) p(b) enqueue V(b) V(f) end loop	loop p(f) p(b) dequeue V(b) V(e) end loop

Which of the following statement is/are true?
1. The purpose of semaphore f is to ensure that dequeue is not executed on an empty queue.
2. The purpose of semaphore e is to ensure the deadlock doesn't occur.
3. The purpose of semaphore b is to provide mutual exclusion for queue operations.

(a) 1 only (b) 2 only
(c) 2 and 3 only (d) 2 and 3 only

3. Peterson's algorithm is the solution of which of the following problem.

(a) Deadlock (b) Mutual exclusion
(c) Thrashing (d) Paging

4. Consider the following code

```
Void main ( )
 {
     …..
for (int k =1 ; k < = 5 ; k + + )
{
pid [k] = for k ( ) ; }
}
```

In the given code all fork ( ) statements execute successfully and all pid vibrations initialized to 0. What will be the total number of processes rated by the above code?

(a) 1 (b) 5
(c) 16 (d) 32

5. Consider the following

```
Int numreader = 0
mutex = semaphore (1) ;
roomempty (1);
```

	Reader Code	Writer Code
r1	Mutex. wait ( ) ;	W roomempty.wait 1 ( );
r2	numreader + - 1;	W_2/*critical writer section&/
r3	if (numreader ==1)	W_3: roomempty signal ();
r4	roomempty.wait ( ) ;	
r5	mutex.signal ( ) ;	
r6	/*critical reader section*/	
r7	mutex.wait();	
r8	numreader - = 1	
r9	if (numreader = = 0)	
r10	roomempty.signal( ) ;	
r11	mutex.signal ( ) ;	

GATE QUESTIONS

1. Which of the following is/are shared by all the threads in a process?

(i) Program counter (ii) Stack
(iii) Address space (iv) Registers

[GATE - 2017]

(a) (i) and (ii) (b) (iii) only
(c) (iv) only (d) (iii) and (iv) only

2. Threads of a process share

[GATE - 2017]

(a) Global variables but not heap
(b) Heap but not global variables
(c) Neither global variable nor heat
(d) Both heap and global variables

3. Consider the following proposed solution for the critical section problem. There are n processes:
P0.....Pn−1. In the code, function pmax returns an integer not smaller than any of its arguments. For all i, t[i] is initialized to zero.

```
Code for Pi:
do {
c[i]=1;
t[i] = pmax(t[0],...,t[n-1])+1; c[i]=0;
for every j □ i in {0,...,n-1}
{
while (c[j]);
while (t[j] != 0 && t[j]<=t[i]);
}
Critical Section;
t[i] = 0;
Remainder Section;
} while (true);
```

Which one of the following is TRUE about the above solution?

[GATE - 2016]

(a) At most one process can be in the critical section at any time
(b) The bounded wait condition is satisfied
(c) The progress condition is satisfied
(d) It cannot cause a deadlock

4. Consider the following two-process synchronization solution.

Process 0
Entry: loop while (turn = = 1);
(critical section)
Exit: turn = 1;
Process 1
Entry: loop while (turn = = 0);
(critical section)
Exit: turn = 0;
The shared variable turn is initialized to zero.
Which one of the following is **TRUE**?

[GATE - 2016]

(a) This is a correct two-process synchronization solution.
(b) This solution violates mutual exclusion requirement.
(c) This solution violates progress requirement.
(d) This solution violates bounded wait requirement.

5. Consider a non-negative counting semaphore S. The operation P(S) decrements S, and V(S) increments S. During an execution, 20 P(S) operations and 12 V(S) operations are issued in some order. The largest initial value of S for which at least one P(S) operation will remain blocked is_____.

[GATE - 2016]

6. The following two functions P1 and P2 that share a variable B with an initial value of 2 execute concurrently.

```
P1( )                P2( )
{ C = B – 1;         { D = 2 * B;
B = 2 * C;           B = D – 1;
}                    }
```

The number of distinct values that B can possibly take after the execution is _____

[GATE - 2015]

7. Two process X and Y need to access a critical section. Consider the following synchronization used by both the processes

CHAPTER - 4
DEADLOCK

4.1 DEADLOCK
It is a situation when a waiting process never again ables to change state, because of unavailability of requested resources, which are held by other waiting process.

4.2 DEADLOCK CHARACTERIZATION
In a deadlock, processes never finish executing, and system resources tied up, preventing other jobs from starting.

4.2.1 Necessary Conditions
1. Mutual exclusion
At least one resource must be held in a non-sharable mode; that is, only one process at a time can use the resource. If another process requests that resource, the requesting process must be delayed until the resources has been released.

2. Hold and wait
A process must be holding at least one resource and waiting to acquire additional resources that are currently being held by other processes.

3. No preemption
Resources cannot be preempted; that is, a resource can be released only voluntarily by the process holding it, after that process has completed its task.

4. Circular wait
A set { P_0, P_1, …, P_n } of waiting process must exist such that P_0 is waiting for a resource held by P_1, P_1 is waiting for a resource held by P_2, and so on …, P_{n-1} and P_n is waiting for a resource held by P_0.

4.2.2 Resource Allocation Graph
(i) It is a directed graph which describes the deadlock.
(ii) It has a set of vertices V and a set of Edges E.
(iii) P is a set of all active processes in the system and R is a set of all resource types in the system.
(iv) Directed edge, let Pi → Rj, signifies that process Pi has required an instance of resource type Rj and is currently waiting for that resource and
Edge Rj → Pi signifies that an instance of resource type Rj has been allocated to process P.
Pi → Rj is called Request Edge and Rj → Pi is called assignment edge.
Pictorially, each process is represented as a circle and each resource type Rj as a rectangle.

4.2.2.1 Diagram of Resource Allocation Graph

ASSIGNMENT

1. A state is safe if the system can allocate resources to each process (up to its maximum) in some order and still avoid deadlock, which of the following is/are true?
1. Deadlock state is unsafe
2. Unsafe state may lead to a deadlock situation
3. Unsafe state must lead to a deadlock situation
4. Deadlock state is a subset of unsafe state

(a) 1 ,2 and 3 (b) 1 and 2 only
(c) 1 ,3 and 4 (d)1 ,2 and 4

2. Match List: I wish List: II select the correct answer using the codes given below the lists:

List - I		List - II	
A	Resource allocation graph	(i)	Right speed devices
B	Signal	(ii)	CPU
C	Bankers algorithm	(iii)	Deadlock detection
D	DMA	(iv)	Interrupt
		(v)	Deadlock avoidance
		(vi)	Monitor

(a) A-iii, B-vi, C-v, D-ii
(b) A-v, B-iv, C-iii, D-i
(c) A-v, B-ii, C-iii, D-i
(d) A-iii, B-iv, C-v, D-i

3. A 2,000-byte file is edited so that its file size is increased to 6,000 bytes. The original location of the file on the hard drive does not contain enough unoccupied space around it to store the entire 6,000 bytes. Which of the following will occur when the file is saved?
(a) The surrounding files will be moved to make room for the larger file
(b) The file will be compressed so that it will fit into the space occupied by the original file
(c) The entire file will be stored in a new location on the hard drive
(d) The file will be stored in segments with pointers linking the nonadjacent sections

4. Why it is not possible to have deadlock involving only a single process?
(a) Because this follows circular-wait condition
(b) Because this follows directly from the hold and wait condition
(c) Because indirectly it follows no-preemption condition
(d) None of these

5. Which of the following resources can cause deadlock?
(a) Printers (b) Shared programs
(c) Read only files (d) All of these

6. With a single resource, deadlock occurs
(a) If there is a single process competing for that resource
(b) If there are more than 2 processes competing for that resource
(c) If there are only two processes competing for that resource
(d) None of these

7. Find truth values (true(T)/false (F)) of the following arguments respectively.
(i) A set of process is deadlock if each process in the set is waiting for an event that only another process in the set can cause.
(ii) An unsafe state means a deadlock state
(iii) A system is in a safe state only if there exists a safe sequence
(iv) In no-preemption condition resource previously grated can be forcibly taken away from a process
(a) TFTT (b) TTFF
(c) TFTF (d) FTTF

8. Find truth values (true (T) /false (F)) of the following statement respectively.
(i) Precedence graph must be acyclic
(ii) Fork instruction provides the means to recombine 2 concurrent computations into one
(iii) Fork instruction must executed atomically
(iv) The result of W (read (a)) is { }

GATE QUESTIONS

1. A multithreaded program P executes with x number of threads and uses y number of locks for ensuring mutual exclusion while operating on share memory locations. All locks in the program are non–reentrant, i.e., if a thread holds a lock *l*, then it cannot re–acquire lock *l* without releasing it. If a thread is unable to acquire a lock, it blocks until the lock becomes available. The minimum value of x and the minimum value of y together for which execution of P can result in a deadlock are:

[GATE - 2017]

(a) x = 1, y = 2 (b) x = 2, y = 1
(c) x = 2, y = 2 (d) x = 1, y = 1

2. A system has 6 identical resources and N processes competing for them. Each process can request atmost 2 resources. Which one of the following values of N could lead to a deadlock?

[GATE - 2015]

(a) 1 (b) 2
(c) 3 (d) 4

3. Consider the following policies for preventing deadlock in a system with mutually exclusive resources.
I. Processes should acquire all their resources at the beginning of execution.
If any resource is not available, all resources acquired so far are released.
II. The resources are numbered uniquely, and processes are allowed to request for resources only in increasing resource numbers.
III. The resources are numbered uniquely, and processes are allowed to request for resources only in decreasing resource numbers.
IV. The resources are numbered uniquely. A process is allowed to request only for resources with resource number larger than its currently held resources.
Which of the above policies can be used for preventing deadlock?

[GATE - 2015]

(a) Any one of I and III but not II or IV
(b) Any one of I, III and IV but not II
(c) Any one of II and III but not I or IV
(d) Any one of I, II, III and IV

4. An operating system uses the Banker's algorithm for deadlock avoidance when managing the allocation of their resource types X, Y, and Z to three processes P0, P1, and P2. The table given below presents the current system state. Here, the Allocation matrix shows the current number of resources of each type allocated to each process and the Max matrix shows the maximum number of resources of each type required by each process during its execution.

	Allocation			**Max**		
	X	Y	Z	X	Y	Z
P0	0	0	1	8	4	3
P1	3	2	0	6	2	0
P2	2	1	1	3	3	3

There are 3 units of type X, 2 units of type Y and 2 units of type Z still available. The system is currently in a safe state. Consider the following independent requests for additional resources in the current state.
REQ1: P0 requests 0 units of X, 0 units of Y and 0 units of Z.
REQ2:P1 requests 2 units of X, 0 units of Y and 0 units of Z.

[GATE - 2014]

(a) Only REQ1 can be permitted.
(b) Only REQ2 can be permitted.
(c) Both REQ1 and REQ2 can be permitted.
(d) Neither REQ1 nor REQ2 can be permitted.

5. A system contains three programs and each requires three tape units for its operation. The minimum number of tape units which the system must have such that deadlocks never arise is _____

[GATE - 2014]

6. A system has n resources R_0, R_1, …., R_{n-1}, and k processes P_0, P_1, ……, P_{k-1}. The

CHAPTER - 5
MEMORY MANAGEMENT

5. MEMORY
It is a system resource, which stores the data and information. To increase CPU performance several processes must be in memory that's why sharing of memory is required. Each word or byte stored in memory has its own address.

5.1 STORAGE RESOURCES
1.Registers
2.Main memory
3.Cache
4.Secondary storage devices

CPU requires its one cycle for accessing registers
Main memory is accessed via transaction on bus and it can take many cycles of CPU in that case the processor needs to halt since it does not have the data required to complete instruction. This situation is unacceptable and to overcome this situation fast memory (cache) is used.

5.2 CONCERNED AREAS OF MEMORY MANAGEMENT
1. Relative speed of accessing physical memory.
2. Correct operation has to protect the operating system from access by user processes.
3. Protect user processes from one another.

To protect access of one process to another, hardware implementation is used.

5.3 HARDWARE ADDRESS PROTECTION WITH BASE AND LIMIT REGISTERS
5.3.1 Base Register
It holds the smallest legal physical memory address for a given process.

5.3.2 Limit Register
It specifies the size of the range.
Protection of memory space is accomplished by having the CPU hardware compares every address generated in user mode with the registers. Any attempt by a program executing in user mode to access operating-system memory or other users' memory results in a trap to the operating system, which treats the attempt as a fatal error (Figure 5.1). this scheme prevents a user program from (accidentally or deliberately) modifying the code or data structures of either the operating system or other users.

ASSIGNMENT

1. An 8 kbyte direct-mapped write-back cache is organized as multiple blocks, each of size 32 byte. The processor generates 32 bit addresses. The cache controller maintains the tag information for each cache block comprising of the following :
1 Valid bit 1 Modified bit
As many bits as the minimum needed to identify the memory block mapped in the cache.
What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?
(a) 4864 bit (b) 6144 bit
(c) 6656 bit (d) 5376 bit

2. A program at the time of executing is called
(a) Dynamic program
(b) Static program
(c) Binded program
(d) A process

3. How many page faults occur for optimal page replacement following reference string, with four page frames?
1, 2, 3, 4, 5, 3, 4, 1, 6, 7, 8, 7,8,9,7,8,9,5,4,5,4,2
(a) 14 (b) 13
(c) 12 (d) 11

4. How many page faults occur in LRU page replacement algorithm for the following reference string, with four page frames?
7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1
(a) 8 (b) 7
(c) 6 (d) 9

5. Which page replacement policy sometimes leads to more page faults when size of memory is increased?
(a) Optimal (b) LRU
(c) FIFO (d) None of these

6. In a paged segmented scheme of memory management, the segment table itself must have a page table because:
(a) The segment table is often too large to fit in one page
(b) Each segment is spread over number of pages
(c) Segment tables point to page table and not to the physical locations of the segment.
(d) The processor's description base register points to a page table

7. A linker is given object modules for a set of programs that were compiled separately. What information need not be include in an object module?
(a) Object code
(b) Relocation bits
(c) Names and locations of all external symbols defined in the object module
(d) Absolute addresses of internal symbols

8. Locality of reference implies that the page reference being made by a process
(a) Will always be to the page used in the previous page reference
(b) Is likely to be one of the pages used in the last few page references
(c) Will always be to one of the pages used in the last few page references
(d) Will always lead to page fault

Linked Data for Q.9 & Q.10
A process refers to 5 pages A,B,C,D and E in the following order A,B,C,D,A,B,E,A,B,C,D,E

9. If the page replacement algorithm is FIFO the number of pages transfer with an empties internal store of 3 frames is
(a) 10 (b) 9
(c) 8 (d) 7

10. If the number of available page frames are increased to 4, then number of page transfer.
(a) Decreases
(b) Increases
(c) Remains the same

GATE QUESTIONS

1. Consider a computer system with 40-bit virtual addressing and page size of sixteen kilobytes. If the computer system has a one-level page table per process and each page table entry requires 48 bits, then the size of the per-process page table is _____ megabytes.

[GATE - 2016]

2. Consider a computer system with ten physical page frames. The system is provided with an access sequence (a_1,a_2,…, a_{20}, a_1, a_2,…a_{20}), where each a_i is a distinct virtual page number. The difference in the number of page faults between the last-in-first-out page replacement policy and the optimal page replacement policy is _____.

[GATE - 2016]

3. In which one of the following page replacement algorithms it is possible for the page fault rate to increase even when the number of allocated frames increases?

[GATE - 2016]

(a) LRU (Least Recently Used)
(b) OPT (Optimal Page Replacement)
(c) MRU (Most Recently Used)
(d) FIFO (First In First Out)

4. Assume that for a certain processor, a read request takes 50 nanoseconds on a cache miss and 5 nanoseconds on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in m cache hit. The average read access time m nanoseconds is _____.

[GATE - 2015]

5. Consider six memory partitions of size 200 KB, 400 KB, 600 KB, 500 KB, 300 KB, and 250 KB, where KB refers to kilobyte. These partitions need to be allotted to four processes of sizes 357 KB, 210 KB, 468 KB and 491 KB in that order. If the best fit algorithm is used, which partitions are NOT allotted to any process?

[GATE - 2015]

(a) 200 KB and 300 KB
(b) 200 KB and 250 KB
(c) 250 KB and 300 KB
(d) 300 KB and 400 KB

6. A Computer system implements 8 kilobyte pages and a 32-bit physical address space. Each page table entry contains a valid bit, a dirty bit three permission bits, and the translation. If the maximum size of the page table of a process is 24 megabytes, the length of the virtual address supported by the system is _____ bits.

[GATE - 2015]

7. Consider a system with byte-addressable memory, 32 bit logical addresses, 4 kilobyte page size and page table entries of 4 bytes each. The size of the page table in the system in megabytes is _____

[GATE - 2015]

8. Consider a main memory with five page frames and the following sequence of page reference: 3, 8, 2, 3, 9, 1, 6, 3, 8, 9, 3, 6, 2, 1, 3. Which one of the following is true with respect to page replacement policies First-In-First Out (FIFO) and Least Recently Used (LRU)?

[GATE - 2015]

(a) Both incur the same number of page faults
(b) FIFO incurs 2 more page faults than LRU
(c) LRU incurs 2 more page faults than FIFO
(d) FIFO incurs 1 more page faults than LRU

9. A computer system implements a 40-bit virtual address, page size of 8 kilobytes, and a 128-entry translation look-aside buffer (TLB) organized into 32 sets each having four ways. Assume that the TLB tag does not store any process id. The minimum length of the TLB tag in bits is _____ .

[GATE - 2015]

CHAPTER - 6
FILE SYSTEM AND DISK SCHEDULING

6.1 INTRODUCTION

1. It is a part of operation system that deals with the management of data storage and data accesses.
2. It is designed to have better performance for disk accesses, preservation of access rights, storage management.
3. It includes what operations are allowed on files ,which data structures are to keep track of free storage, how files are named etc.
4. Generally user view of file system means how a file system appears to a user. It constitutes a file, how they are named, protected and what operations are allowed an files etc.

6.2 FILES

1. It is a way to store information in small units.
2. It has its own name, which consists of two parts:
3. First part denotes the name of file and second part denotes the extension (type) of the file. Both parts of file are separated by dot (·).

1. In MS DOS, file names are 1 to 3 characters.
2. In Unix, the size of the extension is up to the users.
3. Size can have two or more extensions as abc. C.Z where ·Z indicates compressed file and ·c indicate c-program file.

Examples

Extension	Meaning
file·bak	Backup file
file·hlp	help file
file·o	object file
file·ps	Post script file
file·txt	General text file

6.3 FILE STRUCTURE

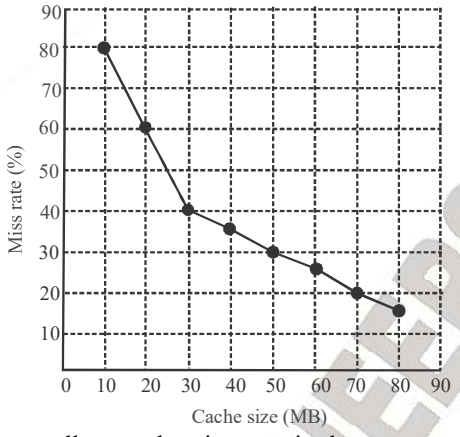
1. Each file has its own structure (means how the records of file are organized)
2. There are three kinds of file structures as Byte sequence, Record sequence, Tree.
3. In unstructured sequence of bytes, operating system sees the file as bytes.
4. In Record sequence, file is a sequence of fixed-length records each with some internal structure.
5. In Tree structure, file consists of a tree of records not necessarily all of the same length each containing same key fields.
6. Following are graphical view of file structures.

GATE QUESTIONS

1. Consider a disk queue with requests for I/O to blocks on cylinders 47, 38, 121, 191, 87, 11, 92, 10.The C-LOOK scheduling algorithm is used. The head is initially at cylinder number 63, moving towards larger cylinder numbers on its servicing pass. The cylinders are numbered from 0 to 199. The total head movement (in number of cylinders) incurred while servicing these requests is_____.

[GATE - 2016]

2. A file system uses an in-memory cache to cache disk blocks. The miss rate of the cache is shown in the figure. The latency to read a block from the cache is 1 ms and to read a block from the disk is 10 ms. Assume that the cost of checking whether a block exists in the cache is negligible. Available cache sizes are in multiples of 10 MB.



The smallest cache size required to ensure an average read latency of less than 6 ms is _____MB.

[GATE - 2016]

3. Consider a typical disk that rotates at 15000 rotations per minute (RPM) and has a transfer rate of 50 × 106 bytes/sec. If the average seek time of the disk is twice the average rotational delay and the controller's transfer time is 10 times the disk transfer time, the average time (in milliseconds) to read or write a 512 byte sector of the disk is _____.

[GATE - 2015]

4. Suppose the following disk request sequence (track numbers) for a disk with 100 tracks is given: 45, 20, 90, 10, 50, 60, 80, 25, 70. Assume that the initial position of the R/W head is on track 50. The additional distance that will be traversed by the R/W head when the Shortest Seek Time First (SSTF) algorithm is used compared to the SCAN (Elevator) algorithm (assuming that SCAN algorithm moves towards 100 when it starts execution) is _____tracks.

[GATE - 2015]

5. Consider a disk pack with a seek time of 4 millisecond and rotational speed of 10000 rotations per minute (RPM). It has 60 sectors per track and each sector can store 512 bytes of data. Consider a file stored in the disk. The file contains 2000 sectors. Assume that every sector access necessitates a seek, and the average rotational latency for accessing each sector is half of the time for one complete rotation. The total time (in milliseconds) needed to read the entire file is _____

[GATE - 2015]

6. A FAT (file allocation table) based file system is being used and the total overhead of each entry in the FAT is 4 bytes is size. Given a 100×10^6 bytes disk on which the file system is stored and data block size is 10^3 bytes, the maximum size of a file that can be stored on this disk in units of 10^6 bytes is_____

[GATE - 2014]

7. Suppose a disk has 201 cylinders, numbered from 0 to 200. At time the disk arm is at cylinder 100, and there is a square of disk access requests for cylinders 30, 85, 90, 100,

SECTION- B
COMPUTER ARCHITECTURE

CHAPTER - 1
BASICS AND ADDRESSING MODE

1.1 INTRODUCTION

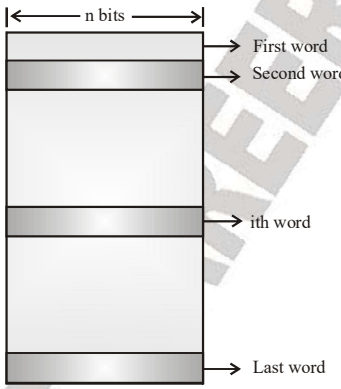
We will first consider how the memory of a computer is organized. The memory consists of many millions of storage cells, each of which can store a bit of information having the value 0 or 1. Because a single bit represents a very small amount of information, bits are seldom handled individually. The usual approach is to deal with them in groups of fixed size.

1.2 MEMORY LOCATIONS AND ADDRESSES

1.The memory is organized so that a group of n bits can be stored or retrieved in a single, basic operation.

2.Each group of n bits is referred to as a word of information, and n is called the word length.

3.The memory of a computer can be schematically represented as a collection of words, as shown in figure.



Memory Words

4.If the word length of a computer is 32 bits, a single word can store a 32-bit signed number or four ASCII-encoded characters, each occupying 8 bits.

5.A unit of 8 bits is called a byte. Machine instructions may require one or more words for their representation.

6.To Access the memory to store or retrieve a single item of information, either a word or a byte, requires distinct names or addresses for each location. It is customary to use numbers from 0 to $(2^k)-1$, for some suitable value of k, as the addresses of successive locations in the memory. Thus, the memory can have up to 2^k addressable locations. The 2^k addresses constitute the address space of the computer.

1.3 BYTE ADDRESSABLE VS WORD ADDRESSABLE

1.3.1 Byte Addressable Memory

Each memory cell points to an 8 bit information.

1.3.2 Word Addressable Memory

Each memory cell points to one word information or size of one word is equal to word length of the processor or the no. of bits processed by the processor at a time.

ASSIGNMENT-I

1. The most appropriate matching for the following pairs
List-I
A. Indirect Addressing
B. Immediate Addressing
C. Auto Decrement Addressing
List-II
(i) Loop
(ii) Pointers
(iii) Constants
Codes:
(a) A-iii, B-ii, C-i
(b) A-i, B-iii, C-ii
(c) A-ii, B-iii, C-i
(d) A-iii, B-i, C-ii

2. Which is the most appropriate match for the items in the first columns with the items in the second column ?
List-I
A. Indirect Addressing
B. Indexed Addressing
C. Base Register Addressing
List-II
(i) Array Implementation
(ii) Writing Relocatable Code
(iii) Passing array as parameter
Codes:
(a) A-iii, B-i, C-ii
(b) A-ii, B-iii, C-ii
(c) A-iii, B-ii, C-i
(d) A-i, B-iii, C-ii

3. Which of the following addressing modes are suitable for program relocation time?
1. Absolute Addressing
2. Based Addressing
3. Relative Addressing
4. Indirect Addressing
(a) 1 and 4 (b) 1 and 2
(c) 1, 2 and 4 (d) 2 and 3

4. Addressing modes are
(a) Explicitly specified
(b) Implied by the instruction
(c) Both (a) and (b)
(d) Neither (a) nor (b)

5. Control circuit designed by _____ tends to have a random structure.
(a) A stable table method
(b) Delay element method
(c) Sequence counter method
(d) None of these

6. Addressing mode facilities access to an operand whose location is defined in relative to the beginning of the data structure in which it appears
(a) Absolute (b) Immediate
(c) Index (d) Indirect

7. Which of the following is displacement addressing mode?
(a) Relative (b) Indexed
(c) Base (d) All of these

8. The most relevant addressing mode is write position independent code is
(a) Direct Mode (b) Indirect Mode
(c) Relative Mode (d) Indexed Mode

9. Which of the following instructions is an example of direct addressing mode?
(a) MOV A, B (b) 2050
(c) 05 (d) HLT

10. Which of the following may not occur in an instruction cycle?
(a) Fetch (b) Decode
(c) Execute (d) Indirect

11. Which of the following instructions requires 1-address space?
(a) 2050 (b) LDA 2010
(c) MOV 05 (d) 1 NRA

12. The following program starts at location 0100 H

GATE QUESTIONS

1. Consider a RISC machine where each instruction is exactly 4 bytes long. Conditional and unconditional branch instructions use PC-relative addressing mode with offset specified in bytes to the target location of the branch instruction. Further the Offset is always with respect to the address of the next instruction in the program sequence. Consider the following instruction sequence

Instr No.	Instruction			
i:	add	R2	R3	R4
i + 1:	sub	R5	R6	R7
i + 2:	cmp	R1	R9	R10
i +3:	beq	R1	offset	

If the target of the branch instruction is i, then the decimal value of the offset is_____.

[GATE - 2017]

2. Consider the C struct defined below:

```
struct data
{   int marks [100];
    char grade;
    int cnumber;
};
Struct data student;
```

The base address of student is available in register R1. The field student. grade can be accessed efficiently using.

[GATE - 2017]

(a) Post-increment addressing mode, (R1) +
(b) Pre-decrement addressing mode, –(R1)
(c) Register direct addressing mode, R1
(d) Index addressing mode. X(R1), where X is an offset represented in 2's complement 16-bit representation.

3. A processor has 40 distinct instruction and 24 general purpose registers. A32-bit instruction word has an opcode, two registers operands and an immediate operand. The number of bits available for the immediate operand field is_____.

[GATE - 2016]

4. Consider a processor with byte-addressable memory. Assume that all registers, including program counter (PC) and Program Status Word (PSW), are size of two bytes. A stack in the main memory is implemented from memory location and It grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is . The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:
1.Store the current value of PC in the stack
2.Store the value of PSW register in the stack
3.Load the starting address of the subroutine in PC . The content of PC just before the fetch of a CALL instruction $(5FA0)_{16}$ is . After execution of the CALL instruction, the value of the stack pointer is

[GATE - 2015]

(a) $(016A)_{16}$ (b) $(016C)_{16}$
(c) $(0170)_{16}$ (d) $(0172)_{16}$

5. Consider two processors
P_1 and P_2executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P_2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on
P_1 If the clock frequency of
P_1 is 1GHZ, then the clock frequency of
P_2 (in GHz) is _____.

[GATE - 2014]

6. Consider a hypothetical processor with an instruction of type, LW R1, 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register.
R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register.
R2. Which of the following best reflects the addressing mode implemented by this instruction for the operand in memory?

[GATE - 2011]

CHAPTER - 2
INSTRUCTION SET

2.1 INTRODUCTION

1.The function of the control unit in a digital computer is to initiate sequences of micro-operations.
2.The complexity of the digital system is derived from the number of sequences of micro-operations that are performed.
3.When the control signals are generated by hardware using conventional logic design techniques, the control unit is said to be hardwired.
4. Microprogramming is a second alternative for designing the control unit of a digital computer.

2.2 MICROINSTRUCTION/MICROPROGRAM

1.In micro programmed control unitech word in control memory contains within it a micro-instruction.
2.The microinstruction specifies one or more micro-operations for the system.
3.A sequence of microinstructions constitutes a micro program. Since alterations of the micro-program are not needed once the control unit is in operation, the control memory can be a read only memory (ROM).

2.2.1 Control Memory

1.The control function specifying a micro operation is a binary variable whose active state could be either 1 or 0.
(i) In the variable's active state, the micro operation is executed.
(ii) The string of control variables which control the sequence of micro operations is called a control word.
2.The micro operations specified in a control word is called a microinstruction. Each microinstruction specifies one or more micro operations that is performed.
3.The control unit coordinates stores microinstruction in its own memory (usually ROM) and performed the necessary steps to execute the sequences of microinstructions (called micro programs).

2.2.2 Control Unit

1.As the name suggests, a control unit is used to control something.
2.The control unit provides instructions to the other CPU devices in a way that causes them to operate coherently to achieve some goal.

2.2.3 Basic Control Unit Operation

1.The basic operation of the CPU is described by the FETCH/DECODE/EXECUTE/ WRITEBACK sequence.
2.The control unit is used to implement this sequence using a micro-program.
3.Instruction Register, Stores the number that represents the machine instruction the Control Unit is to execute.

2.2.4 Control Unit Operations (Execution of the Instruction Cycle)

1.It has many elementary phases, each executed in a single clock cycle.
2.In each phase only very simple operations (called micro-operations) are executed: Move contents between registers (internals, interface with ALU, interface with memory) Activate devices (ALU, memory)

ASSIGNMENT-I

1. Programming that actually controls the path of the data within the computer is called
(a) Micro Programming
(b) System Programming
(c) Assemble Language
(d) Machine Language programming

2. Match the following
List-I
A. Stack overflow
B. Timer
C. Invalid opcode
D. Superior call
List-II
(i) Software interrupt
(ii) Internal interrupt
(iii) External interrupt
(iv) Machine check interrupt
Codes:
(a) A-ii, B-iii, C-ii, D-i
(b) A-ii, B-iii, C-iv, D-i
(c) A-iii, B-i, C-iii, D-iv
(d) None of these

3. The control signal indicates
(a)Whether a data is read into or written out to memory
(b)Whether CPU is accessing memory of input/output device
(c)Whether input/output device or memory is ready to transfer data
(d)All of the above

4. In a microprocessor, the address of the next instruction to be executed, is stored in
(a) Stack pointer
(b) Address latch
(c) Program counter
(d) General purpose register

5. Linkage between CPU and the user is provided by
(a) Peripheral devices
(b) Control unit
(c) Storage
(d) Software

6. The CPU of a computer takes instruction from the memory and executes them. This process is called
(a) Load cycle
(b) Time sequencing
(c) Fetch-execute cycle
(d) Clock cycle

7. An interrupt can be temporarily ignored by the counter is called
(a) Vectored interrupt
(b) Non-maskable interrupt
(c) Maskable interrupt
(d) Low priority interrupt

8. Match List-I with List-II and select the correct answer from the codes given below the lists.
List-I
A. A shift register can be used
B. A mutiplexer can be used
C. A decoder can be used
List-II
(i)For code conversion
(ii)To generate memory chip select
(iii)For parallel to serial conversion
(iv)As many to one switch
(v)For analog to digital conversion
Codes:
(a) A-iii, B-i, C-ii
(b) A-iv, B-iii, C-ii
(c) A-iii, B-iv, C-ii
(d) A-ii, B-iii, C-iv

9. Microprogram is
(a)The name of source program in micro computers
(b)The set of instructions indicating the primitive operations in a system
(c)Primitive form of macros used in assembly language programming
(d)Program of very small size

10. Which of the following units is used to supervise each instruction in the CPU?

GATE QUESTIONS

1. Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is _____.

[GATE - 2016]

2. Suppose the functions F and G can be computed in 5 and 3 nanoseconds by functional units U_F and U_G, respectively. Given two instances of U_F and two instances of U_G , it is required to implement the computation for $F(G(X_i))$ for $1 \le i \le 10$ .Ignoring all other delays, the minimum time required to complete this computation is _____ nanoseconds.

[GATE - 2016]

3. A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is _____

[GATE - 2014]

4. Consider the following sequence of micro-operations.
MBR ← PC MAR ← X PC ← Y Memory ← MBR
Which one of the following is a possible operation performed by this sequence?

[GATE - 2013]

(a) Instruction fetch
(b) Operand fetch
(c) Conditional branch
(d) Initiation of interrupt service

5. A CPU generally handles an interrupt by executing an interrupt service routine

[GATE - 2009]

(a)As soon as an interrupt is raised.
(b)By checking the interrupt register at the end of fetch cycle.
(c)By checking the interrupt register after finishing the execution of the current instruction.
(d)By checking the interrupt register at fixed time intervals.

6. Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125 control signals are needed to be generated by the control unit. While designing the horizontal microprogrammed control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?

[GATE - 2008]

(a) 125, 7 (b) 125, 10
(c) 135, 9 (d) 135, 10

7. Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction size (no. of words)
	MOV R1, (3000)	R1 ←m[3000]	2
LOOP:	MOV R2, (R3)	R2 ← M[R3]	1
	ADD R2, R1	R2 ← R1 + R2	1
	MOV (R3), R2	M[R3] ←R2	1
	INC R3	R3 ←R3 +1	1
	DEC R1	R1← R1 - 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1