GATE 2019

DIGITAL LOGIC

COMPUTER SCIENCE

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Head O ce: S.C.O-121 - 122 - 123, 2nd Floor, Sector-34/A, Chandigarh-160022

Website: www.engineerscareergroup.in **Toll Free:** 1800-270-4242

E-Mail: ecgpublica ons@gmail.com | info@engineerscareergroup.in

GATE-2019: Digital Logic| Detailed theory with GATE previous year papers and detailed solu ons.

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CHAPTER - 1
NUMBER SYSTEM

1.1 DATA REPRESENTATION

Data can be any digit, character or any symbol. And it can be represented in following categories.

Magnitude Representation	Complement Representation
1. Unsigned magnitude representation (positive): No sign bit **2.** Signed magnitude representation (positive, negative): One extra bit (sign) as MSB	**1.** (r–1)'s complement: (positive, negative) **2.** r's complement: (positive, negative) MSB = 0 (positive) MSB = 1 (negative)

1.1.1 Sign Magnitude Representation

1. "+" sign before a number indicates that it is positive (+ve) number and negative (–ve) sign before a number indicates that it is –ve number. Replace +ve with MSB 0 and –ve with MSB 1 followed by binary equivalent of given number to get its sign representation.

2. Range is identical as that of 1's complement and also has 2 unique representation for zero. Its Range = $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$ such as for n = 7 range is (– 63) to (+ 63)

Example

$(+1100101)_2 \rightarrow (01100101)_2$
$(+\ 101.001)_2 \rightarrow (0101.001)_2$
$(-10010)_2 \rightarrow (110010)_2$
$(-110.101)_2 \rightarrow (1110.101)_2$

1.1.2 Complement

There are two types of complements:

1. (r – 1)'s complement

2. (r)'s complement , Where , r = base of complement

- Binary (r = 2)
  - 1's complement
  - 2's complement
- Octal (r = 8)
  - 7's complement
  - 8's complement
- Hexadecimal (r = 16)
  - 15's complement
  - 16's complement
- Decimal (r =10)
  - 9's complement
  - 10's complement

(r–1)'s Complement: To determine this complement, subtract the given number from maximum number having number of digits equal to the number of digits in given number possible in given base.

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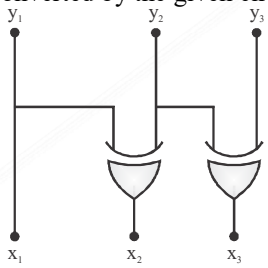
ASSIGNMENT

1. When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero?
(a) sign magnitude (b) 1's complement
(c) 2's complement (d) 9's complement

2. In the following codes a binary number $Y_1Y_2Y_3$ is converted by the given circuit



(a) Excess-3 Code (b) Gray Code
(c) Decimal Code (d) BCD Code

3. Addition of all the gray codes to convert decimal (0-9) into gray code is:
(a) 129 (b) 108
(c) 69 (d) 53

4. Input

(a) + 255 (b) +127
(b) +31 (d) Zero

5. If $(123)_5 = (x3)_y$, then the number of possible values of x is
(a) 4 (b) 3
(c) 2 (d) 1

6. A computer has the following negative numbers stored in binary form as shown. The wrongly stored number is:
(a) –37 as 11011011
(b) –89 as 10100111
(c) –48 as 11101000
(d) –32 as 11100000

7. Octal equivalent of hexadecimal AFAFAF is
(a) 53276757 (b) 76727673
(c) 53727657 (d) 76727672

8. $(177)_8 + 1 = (X)_8$, the value of x is
(a) 178 (b) 179
(c) 200 (d) None of these

9. Noting that $3^2 = 9$, formulate a simple procedure for converting base – 3 numbers directly to base – 9 use the procedure to convert $(2110201102220112)_3$ to base 9.
(a) $(66582614)_9$
(b) $(2206112414)_9$
(c) $(73642815)_9$
(d) None of these

10. Identify the first 10 decimal digits in Base 4 number system
(a) 0, 1, 2, 3, 4, 5, 6, 0, 1, 2
(b) 0, 1, 2, 3, 4, 5, 6, 7, 0, 1
(c) 0, 1, 2, 3, 10, 11, 12, 13, 14
(d) 0, 1, 2, 3, 10, 11, 12, 13, 20, 21

11. What is the 11's complement of $(935)_{12}$?
(a) 124_{11} (b) 234_{10}
(c) 286_{12} (d) 330_{10}

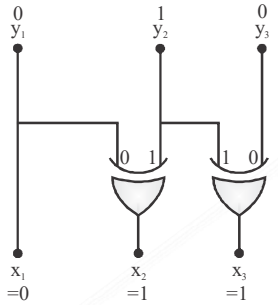
12. X and Y are successive digits in a positional number system. Also $XY = 25_{10}$ and $YX = 31_{10}$. Determine the Radix value of the system and value of X and Y.
(a) 6, 4, 2 (b) 7, 3, 4
(c) 7, 4, 3 (d) 6, 4, 3

13. Consider the signed Binary numbers A = 01000110 and B = 11010011, where B is in 2's complement form. Match the following.
List-I
A. A + B
B. A – B
C. B – A
D. A – B
List-II

SOLUTIONS

Sol. 1 (c)

Sol. 2 (c)



Let us take the binary input 010

∴ It forms a gray code.

Binary Code	Gray Code
000	000
001	001
010	011
011	010
100	110
101	111
110	101
111	100

Sol. 3 (d)

Decimal	BCD	Gray Code	Decimal Equivalent of Gray
0	0000	0000	0
1	0001	0001	1
2	0010	0011	3
3	0011	0010	2
4	0100	0110	6
5	0101	0111	7
6	0110	0101	5
7	0111	0100	4
8	1000	1100	12
9	1001	1101	13
		Total=	+53

Sol. 4 (b)

$X_1 = 1\ 0\ 1\ 0\ 1\ 0\ 1\ 0$, $X_2 = 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$

$X_1 \oplus X_2$=?

X_1	X_2	$X_1 \oplus X_2$
1	1	0
0	1	1
1	1	0
0	1	1
1	1	0
0	1	1
1	1	0
0	1	1

Binary number: $(0\ 1\ 0\ 1\ 0\ 1\ 0\ 1)_2$

Binary to Gray Code: $(0\ 1\ 1\ 1\ 1\ 1\ 1\ 1)_2$

Gray code to Decimal:

$=0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 1 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$

$=64 + 32 + 16 + 8 + 4 + 2 + 1 = +127$

Sol. 5 (c)

$(123)_5 = (x3)_y$ then

$1\times5^2 + 2 \times 5^1 + 3 \times 5^0 = x.y^1 + 3.y^0$

$25 + 10 + 3 = xy + 3$

$35 = xy$

Possible factor of 35 are:

1×35 : when y = 35, x = 1 is possible.

35× 1: when y = 1, x = 35 is not possible

5× 7 : when y = 7, x = 5 is possible.

7 × 5: when y = 5, x = 7 is not possible.

Hence x has 2 possible values.

Sol. 6 (c)

$48_{10} = 00110000$

11001111

$+\ 1$

$-48_{10} = 11010000$

$37_{10} = 00100101$

$1\quad 11011010$

$+\ 1$

$-37_{10} = 11011011$

GATE QUESTIONS

1. Given the following binary number in 32-bit (single precision) IEEE – 754 format:
00111110011011010000000000000000
The decimal value closest to this floating – point number is

[GATE - 2017]

(a) 1.45×10^{1} (b) 1.45×10^{-1}
(c) 2.27×10^{-1} (d) 2.27×10^{1}

2. The representation of the value of a 16- bit unsigned integer X in hexadecimal number system is BCA9. The representation of the value of X in octal number system is

[GATE - 2017]

(a) 57124 (b) 736251
(c) 571247 (d) 136251

3. Let X be the number of distinct 16-bit integers in 2's complement representation. Let Y be the number of distinct 16-bit integers in sign magnitude representation. Then X–Y is_____.

[GATE - 2016]

4. The 16-bit 2's complement representation of an integer is 1111 1111 1111 0101; its decimal representation is _____.

[GATE - 2016]

5. Consider the equation $(43)_x = (y3)_8$ where x and y are unknown. The number of possible solutions are _____.

[GATE - 2015]

6. The number of bytes required to represent the decimal number 1856357 in packed BCD (Binary Coded Decimal) from is _____.

[GATE - 2014]

7. Which of the following is an invalid state in an 8-4-2-1 Binary coded decimal counter

[GATE - 2014]

(a) 1 0 0 0 (b) 1 0 0 1
(c) 0 0 1 1 (d) 1 1 0 0

8. Consider the equation $(123)_5 = (x8)_y$ with x and y as unknown. The number of possible solutions are _____.

[GATE - 2014]

9. The base (or radix) of the number system such that the following equation $\frac{312}{20} = 13.1$ holds is _____.

[GATE - 2014]

10. The decimal value 0.5 in IEEE single precision floating point representation has

[GATE - 2012]

(a) Fraction bits of 000…000 and exponent value of 0
(b) Fraction bits of 000…000 and exponent value of – 1
(c) Fraction bits of 100…000 and exponent value of 0
(d) No exact representation

11. $(1217)_8$ is equivalent to

[GATE - 2009]

(a) $(1217)_{16}$ (b) $(028F)_{16}$
(c) $(2297)_{10}$ (d) $(0B17)_{16}$

12. The two numbers represented in signed 2's complement form are P=11101101 and Q=11100110. If Q is subtracted from P, the value obtained in signed 2's complement form is

[GATE - 2008]

(a)100000111 (b) 00000111
(c)11111001 (d)111111001

13. In the IEEE floating point representation the hexadecimal value 0x00000000 corresponds to

[GATE - 2008]

(a) The normalized value 2^{-127}
(b) The normalized value 2^{-126}
(c) The normalized value + 0
(d) The special value + 0

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CHAPTER - 2
LOGIC GATES & BOOLEAN ALGEBRA

2.1 LOGIC GATE

1. The fundamental building block of digital system Logic gate means that o/p and i/p pattern of gate are assigned logically.

2. The inter connection of Gates is to perform a variety of logical operations is called logic design.

3. The input and output of logic gate can occur only in two levels. These levels are termed as high (1) and Low (0) simply.

4. Truth table show how the logic circuit o/p responds to various combination of logic levels of i/p.

5. There are various types of gates

(i) Basic Gates: NOT, AND & OR

(ii) Universal Gate: NAND & NOR

(iii) EXOR & ENOR: Arithmetic, comparator, code converter, parity generator and parity checker.

2.1.1 Basic Gates

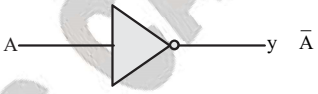
1. NOT Gate

(i) It is one –input and one-output gate.

(ii) Its output is inverted to its corresponding input. If input is 1 then its output is 0 and if its input is 0 then its output is 1.

(iii) It is called inverter.

(iv) It is represented by following symbol

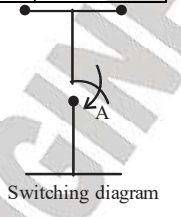


(v) Its all possible input combination and its corresponding output can be represented in the form of table called Truth Table. Truth table for NOT gate is following

Truth Table

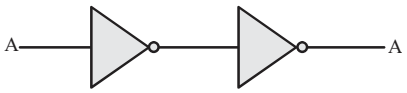
A	y
0	1
1	0

(i)



Switching diagram

(ii)



Buffer Storage

(vi) It act as basic memory element or cross coupled latch storage element and represented as

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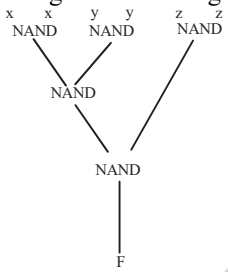
ASSIGNMENT

1. Which of the following logic expression is incorrect?
(a) $1 \oplus 0 = 1$ (b) $1 \oplus 1 \oplus 0 = 1$
(c) $1 \oplus 1 \oplus 1 = 1$ (d) $1 \oplus 1 = 0$

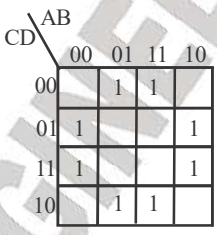
2. Which of the following Boolean algebra statements represent distributive law?
(a) (A+B) +C = A + (B+C)
(b) A. (B+C) = (A.B) + (A.C)
(c) A.(B.C) = (A.B).C
(d) None of these

3. Which expression is computed by the following NAND-gate circuit diagram?



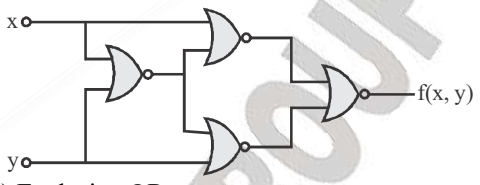
(a) x′y′+z (b) (x+y) z′
(c) x′y′z (d) x′+y′+z′

4. What is the equivalent Boolean expression in product of sum form for the K-map given below?



(a) BD′+B′D
(b) (B+C′+D) (B′+C+D′)
(c) (B+D′) (B′+D)
(d) (B′+D′) (B+D)

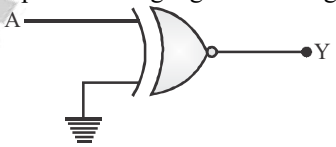
5. Identify the logic function performed by the circuit.



(a) Exclusive OR
(b) Exclusive NOR
(c) NAND
(d) NOR

6. The binary number 110011 is to be converted to gray code. The number of gates and type required are:
(a) 6, AND (b) 6, XNOR
(c) 6, XOR (d) 5, XOR

7. The output of the logic gate in the figure is



(a) AB + AC +BC (b) A +BC
(c) $\overline{A}$ (d) A + B + C

8. What is the minimum number of NAND gates required to implement $A + A\overline{B} + A\overline{B}C$
(a) 0 (b) 1
(c) 4 (d) 7

9. If x and y are Boolean variables, which one of the following is the equivalent of $x \oplus y \oplus xy$.
(a) x+y′ (b) x+y
(c) 0 (d) 1

10. Consider the following gate network which of following gates is redundant?

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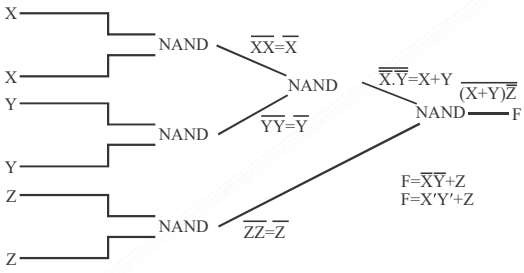
SOLUTIONS

Sol. 1 (b)

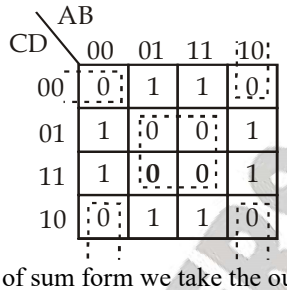
Sol. 2 (a)

Sol. 3 (d)



Hence answer is (a)

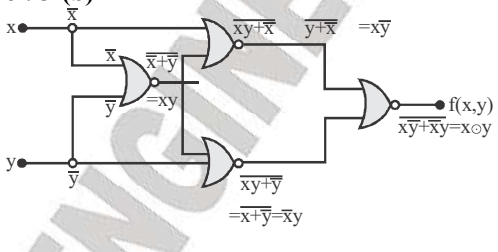
Sol. 4 (d)



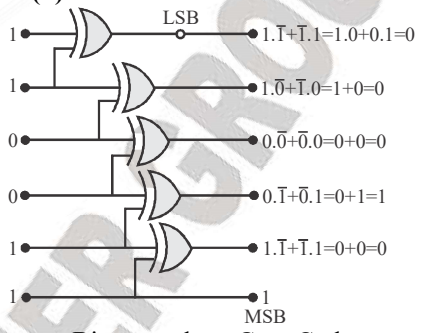
In product of sum form we take the output as 0

$(\overline{B}+\overline{D})(B+D)$

Sol. 5 (b)



Sol. 6 (d)



It converts Binary code to Gray Code.

110011 is converted to 1 0 1 0 1 0

$\therefore$ 5 – XOR gates are required.

Sol. 7 (c)

Ground(G)	A	$G \rightarrow A$
0	0	1
0	1	0

$\therefore$ The Output is complemented.

Sol. 8 (a)

$F = A + A\overline{B} + A\overline{B}C = A + A\overline{B}(1+C)$

$= A + A\overline{B} = A(1+\overline{B})$

$\therefore$ It contains one AND gate and one OR gate, No NAND gate is required.

Sol. 9 (b)

$= x \oplus y \oplus xy = (x\overline{y} + \overline{x}y) \oplus xy$

$= (x\overline{y} + \overline{x}y)\overline{xy} + xy\left[\overline{x\overline{y} + \overline{x}y}\right]$

$= (x\overline{y} + \overline{x}y)(\overline{x} + \overline{y}) + xy\left[xy + \overline{x}\,\overline{y}\right]$

$= x\overline{x}\overline{y} + \overline{x}\,\overline{x}y + x\overline{y}\,\overline{y} + \overline{x}y\overline{y} + (xy.xy) + xy.\overline{x}\,\overline{y}$

$\because \left[A.\overline{A} = 0, A.A = A\right]$

$\therefore\ \overline{x}y + x\overline{y} + xy$

$= \overline{x}y + x(y + \overline{y}) \quad (\because A + \overline{A} = 1)$

(a) $W, Y, XZ, \overline{X}\overline{Z}$ (b) W, Y, XZ

(c) $Y, \overline{X}\overline{Y}\overline{Z}$ (d) $Y, XZ, \overline{X}\overline{Z}$

17. The Boolean expression

$(X+Y)(X+\overline{Y})+(\overline{X\,\overline{Y}})+\overline{X}$ simplifies to

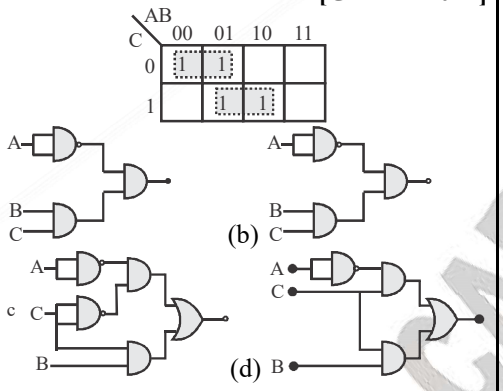
[GATE - 2014]

(a) X (b) Y

(c) XY (d) X+Y

18. Which of the following logic circuits is a realization of the function F whose Karnaugh map is shown in figure.

[GATE - 2014]



19. The SOP (sum of products) form of a Boolean function is $\Sigma(0,1,3,7,11)$, where input are A, B, C, D (A is MSB, and D is LSB). The equivalent minimized expression of the function is

[GATE - 2014]

(a) $(\overline{B}+C)(\overline{A}+C)(\overline{A}+\overline{B})(\overline{C}+D)$

(b) $(\overline{B}+C)(\overline{A}+C)(\overline{A}+\overline{C})(\overline{C}+D)$

(c) $(\overline{B}+C)(\overline{A}+C)(\overline{A}+\overline{C})(\overline{C}+\overline{D})$

(d) $(\overline{B}+C)(A+\overline{B})(\overline{A}+\overline{B})(\overline{C}+D)$

20. Let $\oplus$ denotes the Exclusive OR (XOR) operation. Let '1' and '0' denote the binary constants. Consider the following Boolean expression for F over two variables P and Q.

$F(P, Q) = ((1\oplus P)\oplus(P\oplus Q))\oplus((P\oplus Q)\oplus(Q\oplus 0))$

The equivalent expression for F is

[GATE - 2014]

(a) P + Q (b) $\overline{P+Q}$

(c) $P \oplus Q$ (d) $\overline{P\oplus Q}$

21. Consider the following minterms expression for F:F(P,Q,R,S)=$\sum$(0,2,5,7,8,10,13 ,15) The minterms 2, 7, 8 and 13 are 'do not care' terms. The minimal sum - of - products form for F is

[GATE - 2014]

(a) $Q\overline{S}+\overline{Q}S$

(b) $\overline{Q}\overline{S}+QS$

(c) $\overline{Q}\overline{R}\overline{S}+\overline{Q}R\overline{S}+Q\overline{R}S+QRS$

(d) $\overline{P}\overline{Q}\overline{S}+\overline{P}QS+P\overline{Q}\overline{S}$

22. The dual of a Boolean function $F(x_1, x_2,\ldots x_n,+, \cdot, ')$, written as F^D, is the same expression as that of F with + and · swapped. F is said to be self dual if $F = F^D$. The number of self – dual functions with n Boolean variable is

[GATE - 2014]

(a) 2^n (b) 2^{n-1}

(c) 2^{2^n} (d) $2^{2^{n-1}}$

23. Consider the following Boolean expression for F:

$F(P, Q, R, S) = PQ + \overline{P}QR + \overline{P}Q\overline{R}S$

The minimal sum of products form of F is

[GATE - 2014]

(a) PQ + QR + QS (b) P + Q + R + S

(c) $\overline{P}+\overline{Q}+\overline{R}+\overline{S}$ (d) $\overline{P}R+\overline{P}\overline{R}S+P$

24. Which one of the following expression does NOT represent exclusive NOR of x and y?

[GATE - 2014]

(a) xy + x′y′ (b) $x \oplus y'$

(c) $x' \oplus y$ (d) $x' \oplus y'$

25. In the sum of products function f (X,Y,Z) = $\sum$(2,3,4,5),the prime implications are

[GATE - 2012]

(a) $\overline{X}Y, X\overline{Y}$

(b) $\overline{X}Y, X\overline{Y}\overline{Z}.X\overline{Y}Z$

(c) $\overline{X}Y\overline{Z}, \overline{X}YZ\ XY$

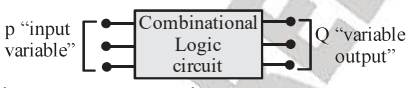
(d) $\overline{X}Y\overline{Z}, \overline{X}YZ, X\overline{Y}\overline{Z}, X\overline{Y}Z$

CHAPTER - 3
COMBINATIONAL LOGIC CIRCUIT

3.1 INTRODUCTION
For any logic Design it is always essential to design a product which meets the requirement as:
1.Minimum cost
2. Minimum space requirement
3. Maximum speed of operations
4. Easy availability of component
5. Ease of inter connection of components
6. Easy to Design

3.1.1 Sequential Logic
Logic circuits whose outputs are determined by the sequence in which input signals are applied.

3.2 COMBINATIONAL CIRCUITS
The circuits whose output depends upon the current input combinations only are called combinational circuits.



Where p is input binary variable term as external source.
And Q is output variable go to external destination.

3.2.1 Design Procedure
1. Statement is assigned with variable analysis.
2. The no. of input and output variable is determined
3. The logic that defined the relation between input and output are determined
4. Logic function diagram is associated

3.2.2 Characteristic of Combinational circuit
1. Present output depends on only the present input
2. No feedback is available/present
3. No storage (many) element is required
Example.
(i) Adder and Subtractor
(ii) Multiplexer and De-Multiplexer
(iii) Decoder and Encoder

3.3 ARITHMETIC COMBINATIONAL CIRCUIT
Adder and Subtractor are Arithmetic combinational circuits.

3.3.1 Half Adder
It adds only any two bits and gives their sum and carry.

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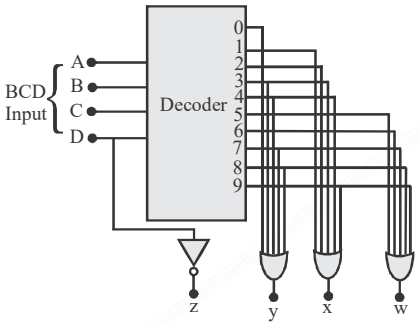
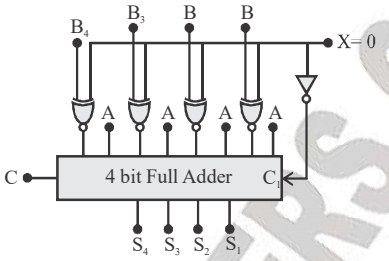
ASSIGNMENT

1. The following logic circuit f(w, x, y, z) indicates



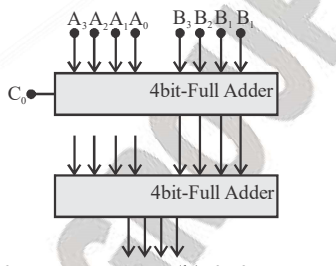
(a) Binary to BCD converter
(b) BCD to Binary converter
(c) BCD to Decimal converter
(d) BCD to Excess – 3 converter

2. Identify the function of the following logic circuit



(a) 4 – bit Binary adder
(b) 4 – bit BCD Adder
(c) 4 – bit Binary subtractor
(d) 4 – bit BCD subtractor

3. The following logic circuit adds two digits represented in the Excess - 3 code. The correction required after adding the two digits in EX-3 form is as follows.
If $C_0 = 1$ and + 3
Identify the inputs to be given to the 2^{nd} 4 - bit full adder?



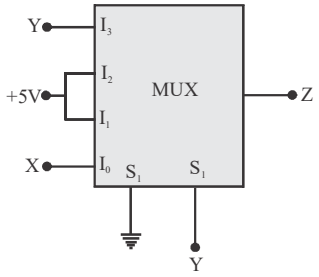
(a) $C_0, C_0, 0, C_0$ (b) $0, 0, C_0, C_0$
(c) $0, 0, C_0, C_0$ (d) $\overline{C}_0, \overline{C}_0, \overline{C}_0, 1$

4. A Boolean function F with A, B, C as inputs is expressed on Karnaugh map as shown below. If this function is implemented with 4 : 1 multiplexer as B, C selection lines, identify the input connections

A \ BC	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$			1	
A	1	1		1

(a) A, A, $\overline{A}$, 1 (b) A, A, 1, $\overline{A}$
(c) A, 1, $\overline{A}$, 0 (d) A, A, $\overline{A}$, A

5. The output of the 4 × 1 multiplexer shown in figure is



(a) $X + Y$ (b) $\overline{X}\overline{Y} + X$
(c) $X\overline{Y}$ (d) $\overline{X} + \overline{Y}$

6. Identify the output of the following logic circuit

SOLUTIONS

Sol. 1 (d)
From truth table of BCD to excess – 3 code
$z = \overline{D}$
$y = \sum m(0,3,4,7,8)$
$x = \sum m(1,2,3,4,9)$
$w = \sum m(5,6,7,8,9)$

Sol. 2 (c)
It is 4 – bit binary subtractor

Sol. 3 (d)
If $C_0 = 1$ and 3 means i/p to 2nd 4 – bit full adder should be 0011 $\Rightarrow \overline{C}_0\overline{C}_0C_0 1$
If $C_0 = 0$ subtract 3 means i/p to 2nd 4 – bit full adder should be 1101 $\Rightarrow \overline{C}_0\overline{C}_0C_0 1$ So i/p to 2nd adder should be $\overline{C}_0\overline{C}_0C_0 1$.

Sol. 4 (d)
From K – map

A \ BC	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	0	0	1	0
A	1	1	0	1

When BC = 00, o/p is equal to A, so $I_0 = A$
When BC = 01, o/p is equal to A, so $I_1 = A$
When BC = 10, o/p is equal to A, so $I_2 = A$

Sol. 5 (a)
$Z = Y + \overline{Y}X$
$= (Y + \overline{Y})(X + Y) = X + Y$

Sol. 6 (a)
$F = \overline{X}_1\overline{X}_2 + X_1X_2 = X_1 \odot X_2$

Sol. 7 (d)
For full adder Sum = A ⊕ B ⊕ C and
Carry = AB + C (A ⊕ B)
So it requires 2 2 input X-OR , 2 input AND 1,2 2 input OR gates.

Sol. 8 (c)
For Sum = 20 + 20 = 40ns
For Carry = 20 + 10 + 10 = 40ns

Sol. 9 (b)
$X = [(A \oplus B)C] + [(AB) \oplus C]$
$= (A\overline{B} + \overline{A}B)C + AB\overline{C} + \overline{AB}C$
$= A\overline{B}C + \overline{A}BC + AB\overline{C} + \overline{A}C + \overline{B}C$

Sol. 10 (c)
$X = \overline{A}C + \overline{B}C + B\overline{C}$
So there are 5 literal $\overline{A}, \overline{B}, C, B$ and $\overline{C}$

Sol. 11 (c)
O/P of AND gate is (x y) $(x\overline{y}) = 0$
$F = D_0 + D_1 = \overline{O}\overline{A}_0 + \overline{O}A_0 = \overline{O} = 1$

Sol. 12 (c)
Output of first MUX $= \overline{b}\overline{a} + ab = a \odot b$
$Z_1 = \overline{c}\overline{(a \odot b)} + (a \odot b)c$
$= a \odot b \odot c$
$Z_2 = \overline{(a \odot b)}b + (a \odot b)c$
$= (a\overline{b} + \overline{a}b)b + (ab + \overline{a}\overline{b})c$
$= \overline{a}b + abc + \overline{a}\overline{b}c$
$= \overline{a}b + bc + \overline{a}c$

Sol. 13 (b)
$Y = \overline{A}0 + AB = AB$

Sol. 14 (d)
To construct a 5 × 32 line decoder 11 1-to-4 decoders are used.

Sol. 15 (a)
For C_5 generation, 4 carry generation path will come into path.

Sol. 16 (c)
Total delay = 31 × 12 + 42 = 414 ns

Sol. 17 (c)

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GATE QUESTIONS

1. When two 8-bit numbers A_7 ….. A_0 and B_7 ….B_0 in 2's complement representation (with A_0 and B_0 as the least significant bits) are added using a ripple - carry adder, the sum bits obtained are S_7….. S_0 and the carry bits are C_7…… C_0 . an overflow is said to have occurred if

[GATE - 2017]

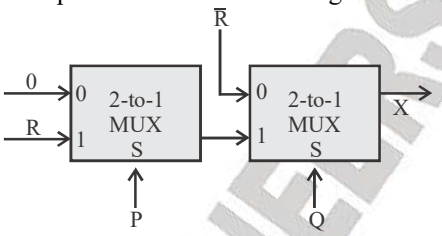
(a) The carry bit C_7 is 1
(b) All the carry bits (C_7 , …… , C_0) are 1
(c) $(A_7.B_7.\overline{S}_7 + \overline{A}_7.-\overline{B}_7.S_7)$ is 1
(d) $(A_0.B_0.\overline{S}_0 + \overline{A}_0.-\overline{B}_0.S_0)$ is 1

2. Consider a carry look ahead adder for adding two n-bit integers, built using gates of fan-in at most two. The time to perform addition using this adder is

[GATE - 2016]

(a) Θ(1) (b) Θ(log(n))
(c) Θ(n) (d) Θ(n)

3. Consider the two cascaded 2-to-1 multiplexers as shown in the figure.



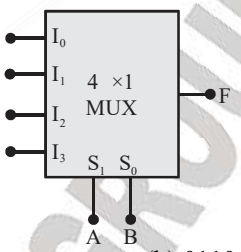
The minimal sum of products form of the output X is

[GATE - 2016]

(a) P Q + P′Q′R (b) PQ+QR
(c) PQ′ + P′QR (d) Q′R′ + PQR

4. In the 4 × 1 multiplexer, the output F is given by F = A ⊕ B. Find the required input '$I_3I_2I_1I_0$'.

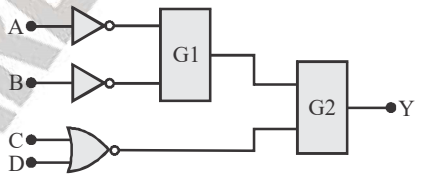
[GATE - 2015]



(a) 1010 (b) 0110
(c) 1000 (d) 1110

5. In the figure shown, the output Y is required to be $Y = AB + \overline{C}\,\overline{D}$. The gates G1 and G2 must be, respectively

[GATE - 2015]



(a) NOR, OR (b) OR, NAND
(c) NAND, OR (d) AND, NAND

6. A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using full adders. The total propagation time of this 4-bit binary adder in microseconds is _____.

[GATE - 2015]

7. The number of min-terms after minimizing the following Boolean expression is _____
[D′ + AB′ + A′C + AC′D + A′C′D]′

[GATE - 2015]

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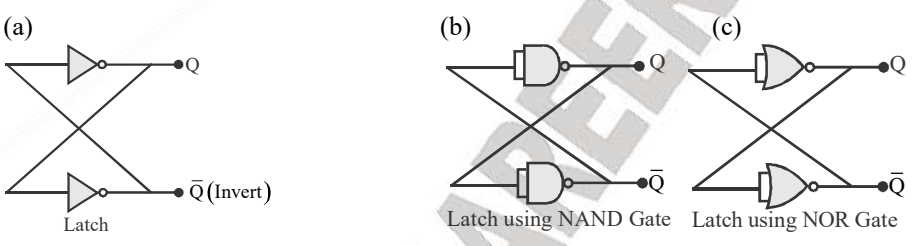
CHAPTER - 4
SEQUENTIAL LOGIC CIRCUIT

4.1 INTRODUCTION

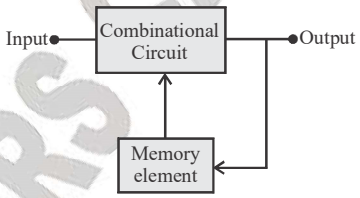
1. In combinational circuit the present O/P depends only upon the present input any prior level. (Input condition) does not have any effect on present output.
2. In sequential circuits, Present output depends upon the present input combinations as well as previous outputs of the system. Therefore, sequential circuits have feedback property.

4.2 1-BIT MEMORY CELL

1. The following circuits are designed to store 1-bit data. They use feedback property hence they are sequential circuits that are the simplest.**2.** Information stored in memory element at any given time define the present state of sequential circuit.

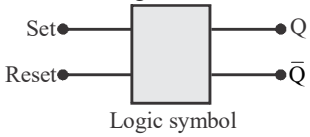


Block Diagram



4.3 LATCHES

1. It refers to unclocked flip flop because these flip flop latch on to a "1" or a "0" Imperially upon running the input called "SET" and "RESET".
2. They are not dependent upon the clock signal for their operation.
3. A latch is a sequential device that checks all its inputs continuously and changes its output accordingly at any time independent of clock signals.



4.3.1 S-R Latch using NOR Gate

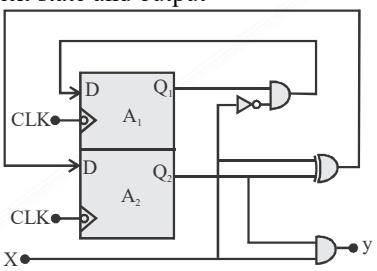
The Set – Reset Latch can be designed using NOR Gates as following

ASSIGNMENT

1. A counter constructed using T – FFs counts the decimal digits according to 2, 4, 2, 1 code. The input T_B is

(a) A′ B + CD (b) A′ B + BCD
(c) A′ B + D (d) A′ B + A′ D

2. A sequential circuit is as shown below. If present states of A_1, A_2, are 1, 0 and x = 1, what is its next state and output

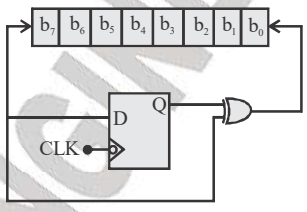


(a) 0, 1, 0 (b) 1, 0, 0
(c) 0, 1, 1 (d) 1, 1, 1

3. In a 4 bit modulo – 6 ripple counter the proportional delay of J-K Flip flop is 50ns. What is the max clock frequency that can used without skipping a count ?

(a) 2MHz (b) 4 MHz
(c) 5 KHz (d) 5 MHz

4. In the following logic circuit, the 8 bit left shift register and D – Flip flop is synchronized with same clock. The D – Flip flop is initially cleared. The circuit acts as



(a) Binary to 2′s complement converter
(b) Binary to EX – 3 code converter
(c) Binary to 1′s complement converter
(d) Binary to Gray code converter

5. A N – bit register is constructed using D – flip – flops. Match the following List-I with List-II

List-I

A. Parallel in parallel out
B. Serial in serial out
C. Parallel in serial out
D. Serial in parallel out

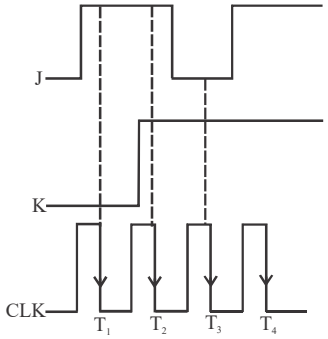
List-II

(i) (2N – 1) clock pulses
(ii) One clock pulses
(iii) N clock pulses
(iv) (N – 1) clock pulses

Codes:

(a) A-iii, B-iv, C-ii, D-i
(b) A-iv, B- ii, C-i, D-iii
(c) A-iii, B-ii, C-iv, D-i
(d) A-ii, B-i, C-iv, D-iii

6. Determine the output of the negative Edge triggered J-K flip flop for the following input waveforms at T_1, T_2, T_3, T_4. Assume the hold time FF is 0.



(a) 0, 1, 0, 1 (b) 0, 1, 1, 0
(c) 1, 0, 0, 1 (d) 1, 0, 1, 1

7. Two J – K FFS having negative edge triggering are connected as shown in figure. Which of the following conditions have to be satisfied for proper functioning of the circuit .

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SOLUTIONS

Sol. 1 (a)

Decimal	Present State $Q_AQ_BQ_CQ_D$	Next State $Q_A^+Q_B^+Q_C^+Q_D^+$	$T_AT_BT_CT_D$
0	0 0 0 0	0 0 0 1	0 0 0 1
1	0 0 0 1	0 0 1 0	0 0 1 1
2	0 0 1 0	0 0 1 1	0 0 0 1
3	0 0 1 1	0 1 0 0	0 1 1 1
4	0 1 0 0	1 0 1 1	0 1 1 1
5	1 0 1 1	1 1 0 0	0 1 0 1
6	1 1 0 0	1 1 0 1	0 0 0 1
7	1 1 0 1	1 1 1 1	0 0 1 1
8	1 1 1 0	1 1 1 0	0 0 0 1
9	1 1 1 1	1 1 1 1	1 1 1 1

T_B

AB \ CD	00	01	11	10
00	0	1	1	1
01	1	×	×	×
11	0	0	1	0
10	×	×	1	×

Sol. 2 (c)
Input to A_1 D F/F = 0
Input to A_2 D F/F = 1
so after clock o/p of A_1 and A_2 will be 0, 1 respectively so y = 1.

Sol. 3 (d)
Total propagation delay = 4 × 50 ns
maximum frequency used

$$= \frac{1}{200 \times 10^{-9}} = 5 \times 10^6 \text{ Hz}$$

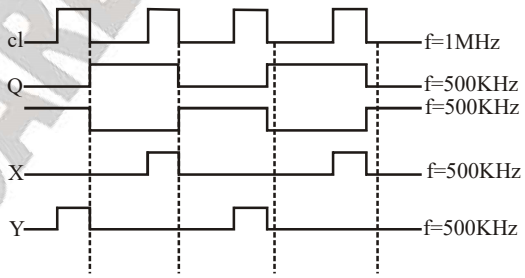
Sol. 4 (d)
Circuit act as binary to gray code convertor

Sol. 5 (d)
Parallel In Parallel out – one clock pulse
Serial in Serial out – (2N – 1) clock pulses
Parallel in serial out – (N – 1) clock pulses
Serial in parallel out – N clock pulses

Sol. 6 (b)
For T_1, J = 1 and K = 0, so Q = 1
For T_2, J = 1 and K = 0, so Q = 0
For T_3, J = 0 and K = 1, so Q = 0
For T_4, J = 1 and K = 1, so Q = 1

Sol. 7 (c)
For proper functioning $t_h < t_{PLH}$, so that 2nd FF can latch proper data.

Sol. 8 (d)
X = Q clock and Y = $\overline{Q}$ clock
So waveforms are as follows



Sol. 9 (c)
Using 3FF counter can count 2^3 = 8 states Therefore, mod – 6 counter will slip 2 counts if it is made of 3FF.

Sol. 10 (d)
When X = $\overline{B}$ and Y = $\overline{C}$, the outputs are cleared at the sequence CBA = 110. For all other states, the counter works in normal operation.

Sol. 11 (a)
For m FF total no. of outcomes (outputs) will be 2m and total number of inputs = n (given). Hence in state table total columns will be total o/p's + total no. of i/p's = 2m +n

Sol. 12 (d)

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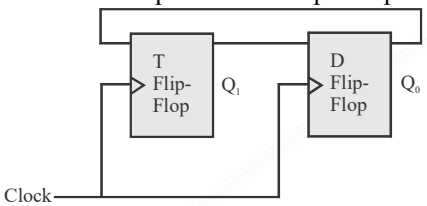
GATE QUESTIONS

1. Consider a combination of T and D flip – flops connected as shown below. The output of the D flip – flop is connected to the input of the T flip – flop and the output of the T flip – flop is connected to the input of the D flip – flop.



Initially, both Q_0 and Q_1 are set to 1 (before the 1st clock cycle). The outputs

[GATE - 2017]

(a) Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 00 respectively
(b) Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 00 respectively
(c) Q_1Q_0 after the 3rd cycle are 00 and after the 4th cycle are 11 respectively
(d) Q_1Q_0 after the 3rd cycle are 01 and after the 4th cycle are 01 respectively

2. The next state table of a 2-bit saturating up – counter is given below.

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using T flip – flops. The expression for T_1 and T_0 are

[GATE - 2017]

(a) $T_1 = Q_1Q_0, T_0 = \overline{Q_1}\,\overline{Q_0}$
(b) $T_1 = \overline{Q_1}Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$
(c) $T_1 = Q_1 + Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$
(d) $T_1 = \overline{Q_1}Q_0, T_0 = Q_1 + Q_0$

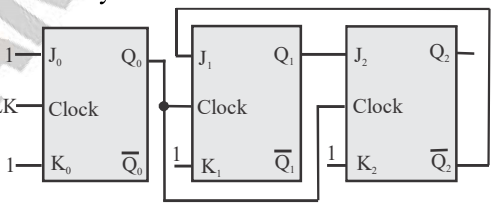
3. We want to design a synchronous counter that counts the sequence 0-1-0-2-0-3 and then repeats. The minimum number of J-K flip-flops required to implement this counter is _____.

[GATE - 2016]

4. Consider an eight-bit ripple-carry adder for computing the sum of A and B, where A and B are integers represented in 2's complement form. If the decimal value of A is one, the decimal value of B that leads to the longest latency for the sum to stabilize is_____.

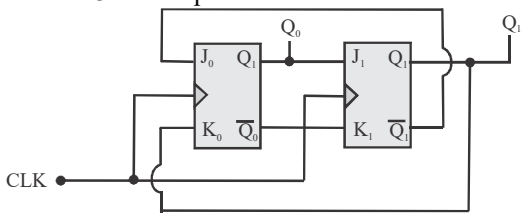
[GATE - 2016]

5. The figure shows a digital circuit constructed using negative edge triggered J – K flip flops. Assume a starting state of $Q_2Q_1Q_0 = 000$. This state $Q_2Q_1Q_0 = 000$ will repeat after _____ number of cycles'.



[GATE - 2015]

6. In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is $Q_1Q_0 = 00$. The state (Q_1Q_0), immediately after the 3rd clock pulse is



[GATE - 2015]

(a) 00 (b) 01
(c) 10 (d) 11

7. The figure shows a binary counter with synchronous clear input. With the decoding logic shown, the counter works as a