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# CHAPTER - 1
# *SEMICONDUCTOR PHYSICS*

## 1.1 DE BROGLIE'S Concept of Matter Waves

According to DE BROGLIE'S hypothesis a moving particle is associated with a wave called De Broglie wave. The wavelength of matter wave is given by:

$$\lambda = \frac{h}{mv} = \frac{h}{p}$$

h is Plank's constant = $6.64 \times 10^{-34}$ Joules / sec

mass of electrons = $9.1 \times 10^{-31}$ kg

v is velocity of moving particle

p is momentum of electron

## 1.2 ENERGY BANDS IN SOLIDS

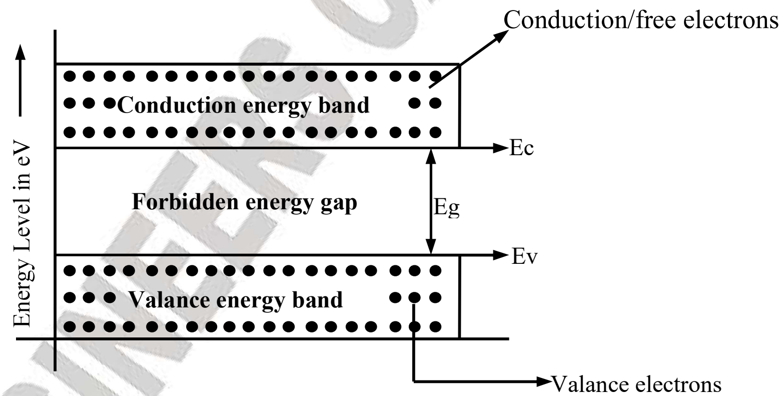
1. Forbidden energy gap
2. Valance band
3. Conduction band

### 1. Forbidden Energy Gap

The separation between the conduction band and valance band is known as forbidden energy gap. In this region no electrons are present.

### 2. Valance Band

**It is d**efined as a band which is occupied by valance electrons or a band having highest occupied band energy.




**Representation of Bands**

If sufficient energy is given to electrons in valance band, some of free electrons left valance band which are responsible for conduction of current.

### 3. Conduction Band

It is defined as the lowest unfilled energy band. Electrons from valance band reach the conduction band, called as conduction electrons; they form conduction of current in conductor.

# WORKBOOK

**Example 1.** Two semiconductor materials have exactly the same properties except that material A has a band gap of 1.0 eV and material B has a band gap energy of 1.2 eV. The ratio of intrinsic concentration of material A to that of material B is

(a) 2016 (b) 47.5
(c) 58.23 (d) 1048

**Solution.**

$$\frac{n_{iA}^2}{n_{iB}^2} = \frac{e^{\frac{-EgA}{kT}}}{e^{\frac{-EgB}{kT}}} = e^{-\frac{EgA+EgB}{kT}}$$

$$= e^{-\left[\frac{1-102}{0.026}\right]} = 2257.5$$

$$\Rightarrow \frac{n_{iA}^2}{n_{iB}^2} = 2257.5 \quad \Rightarrow \frac{n_{iA}}{n_{iB}} = 47.5$$

**Example 2.** Find the numerical value of effective density of state function in the conduction band for a semiconductor with effective mass of an electron is 1.5 times the mass of free electrons i.e. 1.5 $m_o$, where $m_o$ is the mass of free electrons.

**Solution.**

$$m_e = 1.5 m_o$$

$$m_o = 9.1\times10^{-31}\ \text{kg}$$

$$\therefore m_e = 1.5\times9.1\times10^{-31}$$

$$= 13.65\times10^{-31}\ \text{kg}$$

$$T = 300\,\text{K}$$

$h$ = planks constant

$$= 6.64\times10^{-34}\ \text{J/sec}$$

$$\bar{k} = 1.38\times10^{-23}\ \text{Joules}/^\circ\text{K}$$

$$N_i = 2\left(\frac{2\pi m_e \bar{k}T}{h^2}\right)^{3/2}$$

$$= 2\left[\frac{2\pi\times13.65\times10^{-31}\times1.38\times10^{-23}\times300}{(6.64\times10^{-34})^2}\right]^{3/2}$$

$$N_c = 4.57\times10^{19}/\text{cm}^3$$

**Example 3.** A silicon sample is uniformly doped with $10^{16}$ phosphorus atoms/cm$^3$ and $2\times10^{16}$ boron atoms/cm$^3$. If all the dopants are fully ionized, the material is of which type and what is its carrier concentration?

**Solution.**

Phosphorus atoms concentration

$n \cong N_D = 10^{16}$ atoms/cm$^3$.

Boron atoms concentration $p \cong N_A = 2\times10^{16}$ atoms/cm$^3$

$$\therefore N_A >> N_D$$

$\therefore$ p-type with carrier concentration of $N_A - N_D = 10^{16}/\text{cm}^3$

**Example 4.** Intrinsic carrier concentration of silicon (energy band gap is 1.12 eV at 300 K) is $1.5\times10^{10}/\text{cm}^3$. Calculate $n_i$ at 400 K. Given that $k = 8.62\times10^{-5}\ \text{eV}/^\circ\text{K}$.

**Solution.**

**Case-1.** at 300 K

$$n_i^2 = AT^3 e^{-\frac{Eg}{kT}}$$

$$n_i^2 = A(300)^3 e^{-\frac{1.12}{8.62\times10^{-5}\times300}}$$

$$n_i^2 = A(27\times10^6)e^{-43} \qquad \text{...(i)}$$

**Case-2.** at T = 400 K

$$n_{i1}^2 = A(400)^3 e^{-\frac{1.12}{8.62\times10^{-5}\times400}}$$

$$n_{i1}^2 = A(64\times10^6)e^{-32} \qquad \text{...(ii)}$$

From (i) and (ii)

$$\frac{n_i^2}{(27\times10^6)e^{-43}} = \frac{n_{i1}^2}{(64\times10^6)e^{-32}}$$

$$n_{i1}^2 = \frac{n_i^2\times(64\times10^6)e^{-32}}{(27\times10^6)e^{-43}}$$

$$= \frac{(1.5\times10^{10})^2(64\times10^6)e^{-32+43}}{(27\times10^6)}$$

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# ASSIGNMENT

**1.** Mobility is 36 $m^2$ / (Vs) and carrier life time 340 μs. The diffusion length is:
(a) 3.13 mm (b) 1.77 mm
(c) 3.55 mm (d) 3.13 mm

**2.** The hall constant in a p-Si bar is given by $5\times10^3$ $cm^3$/ coulomb. The hole concentration in the bar is given lay:
(a) $1.00 \times 10^{15}/cm^3$ (b) $1.25 \times 10^{15}/cm^3$
(c) $1.50 \times 10^{15}/cm^3$ (d) $1.6 \times 10^{15}/cm^3$

**3.** The resistivity at room temperature of intrinsic silicon is $2.3 \times 10^3$ Ω m and that of an n-type extrinsic silicon sample is $8.33 \times 10^{-2}$ Ω m. A bar of this extrinsic silicon 50×100 mm and a steady current of 1μA exists in the bar. The voltage across the bar is found to be 50mV. If the same bar is of intrinsic silicon, the voltage across the bar will be about
(a) 1400 V (b) 140 V
(c) 14 V (d) 1.4 V

**4.** The free $e^-$ density in a conductor is $(1/1.6)\times10^{22}$ $cm^{-3}$ The $e^-$ mobility is 10 $cm^2$/Vs. What is the value of its resistivity.
(a) $10^{-4}$ Ω m (b) $1.6\times10^{-2}$ Ω m
(c) $10^{-4}$ Ω cm (d) $10^4$ mho $cm^{-2}$

**5.** The intrinsic concentration in a semi conductor at 300 K is $10^{13}$ $cm^{-3}$. When it is doped with donor type impurities, the majority carrier density?
(a) $0.999\times10^{17}$ $cm^{-3}$ (b) $10^{17}$ $cm^{-3}$
(c) $10^4$ $cm^{-3}$ (d) $10^9$ $cm^{-3}$

**6.** Two pure specimen of a semiconductor material are taken. One is doped with $10^{18}$ $cm^{-3}$ number of donors and the other is doped with $10^{16}$ $cm^{-3}$ numbers of acceptors. The minority carrier density in the first specimen is $10^7$ $cm^{-3}$. What is the minority carrier density in the other specimen?
(a) $10^{16}$ $cm^{-3}$ (b) $10^{27}$ $cm^{-3}$
(c) $10^{18}$ $cm^{-3}$ (d) $10^9$ $cm^{-3}$

**7.** Under high electric fields, in a semiconductor with increasing electric field.
(a) The mobility of the charge carriers decreases
(b) The mobility of charge carriers increases
(c) The velocity of charge carriers saturates
(d) The velocity of charge carriers increases

**8.** An n type silicon sample, having electron mobility is twice the hole mobility, $\mu_P$ is subjected to a steady illumination such that the $e^-$concentration doubles from its thermal equilibrium value. As a result, the conductivity of the sample increases by a factor of
(a) $2^0$ (b) $2^1$
(c) $5^1$ (d) $4^1$

**9.** In an n- type silicon crystal at room temperature which of the following can have a concentration of $4\times10^{19}$ $cm^{-3}$?
(a) Silicon atoms (b) Holes
(c) Dopant atoms (d) Valence $e^-$s.

**10.** The ratio of the mobility to the diffusion coefficient in a semiconductor has the units
(a) $V^{-1}$ (b) $Cm/V^{-1}$
(c) $V/cm^{-1}$ (d) $V^{-5}$

**11.** A silicon p–n junction at a temperature of $20^0$ C has a reverse saturation current of 10 PA. The reverse saturation current at $40^0$ C for the same bias is approximately:
(a) 30 PA (b) 40PA
(c) 50PA (d) 60PA

**12.** The concentration of minority carriers in an extrinsic semiconductor under equilibrium is
(a) Directly proportional to the doping concentration



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# GATE QUESTIONS

**1.** A solar cell of area 1.0 $cm^2$, operating at 1.0 sun intensity, has a short circuit current of 20 mA, and an open circuit voltage of 0.65 V. Assuming room temperature operation and thermal equivalent voltage of 26 mV, the open circuit voltage (in volts, correct to two decimal places) at 0.2 sun intensity is _______

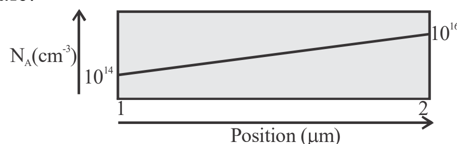
**[GATE - 2018]**

**2.** A bar of Gallium Arsenide (GaAs) is doped with Silicon such that the Silicon atoms occupy Gallium Arsenic sites in the GaAs crystal. Whicho one of the following statements is true?

**[GATE - 2017]**

(a) Silicon atom act as p-type dopants in Arsenic sites and n-type dopants in Gallium sites
(b) Silicon atoms act as n-type dopants in Arsenic sites and p-type dopants in Gallium sites
(c) Silicon atoms act as p-type dopants in Arsenic sites as well as Gallium sites
(d) Silicon atoms act as n-type dopants in Arsenic sites as well as Gallium sites

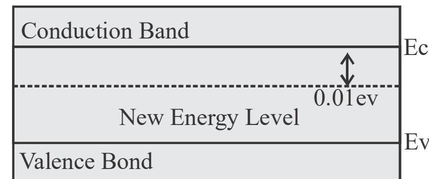
**3.** The figure below shows the doping distribution in a P-type semiconductor in log scale.




The magnitude of the electric field (in kV/cm) in the semiconductor due to non uniform doping is_____.

**[GATE - 2016]**

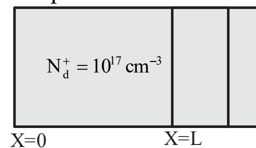
**4.** A small percentage of impurity is added to intrinsic semiconductor at 300 K. Which one of the following statements is true for the energy band diagram shown in the following figure?




**[GATE - 2016]**

(a)Intrinsic semiconductor doped with pentavalent atoms to form n-types semi-conductor
(b) Intrinsic semiconductor doped with trivalent atoms to form n-types semiconductor
(c)Intrinsic semiconductor doped with pentavalent atoms to form p-types semi-conductor
(d) Intrinsic semiconductor doped with trivalent atoms to form p-type semiconductor

**5.** Consider a region of silicon denote of electrons and holes, with an ionized donor density of $N_d^+ = 10^{17} cm^{-3}$ . The electric filed at x = 0 is 0 V/cm and the electric filed at x = L is 50 kV/cm in the positive x direction. Assume that the electric filed is zero in the y and z directions at all points.




Given q = $1.6 \times 10^{-19}$ coulomb, $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm, $\varepsilon_r = 11.7$ for silicon, the value of L in nm is __________.

**[GATE - 2016]**

**6.** A silicon bar is doped with donor impurities $N_D = 2.25 \times 10^{15}$ atoms /$cm^3$. Given the intrinsic carrier concentration of silicon at T = 300K is $n_i = 1.5 \times 10^{10}$ $cm^{-3}$. Assuming complete impurity ionization, the equilibrium electron and hole concentrations are

**[GATE - 2014]**

(a) $n_0 = 1.5 \times 10^{16}$ $cm^{-3}$, $p_0 = 1.5 \times 10^5$ $cm^{-3}$
(b) $n_0 = 1.5 \times 10^{10}$ $cm^{-3}$, $p_0 = 1.5 \times 10^{15}$ $cm^{-3}$

# ESE OBJ QUESTIONS

**1.** Silicon devices can be employed for a higher temperature limit (190 °C to 200 °C) as compared to germanium devices (85°C to 100°C). With respect to this, which of the following are incorrect?
1. higher resistivity of silicon
2. Higher gap energy of silicon
3. Lower intrinsic concentration of silicon
4. Use of silicon devices in high – power applications

Which of the above statements are correct?

**[EC ESE - 2018]**

(a) 1, 2 and 4 (b) 1, 2 and 3
(c) 1, 3 and 4 (d) 2, 3 and 4

**2.** A sample of germanium is made p-type by addition of indium at the rate of one indium atom for every $2.5 \times 10^8$ germanium atoms. Given, $n_i = 2.5 \times 10^{19}$ /m$^3$ at 300 K and the number of germanium atoms per m$^3$ = $4.4 \times 10^{28}$. What is the value of $n_p$?

**[EC ESE - 2018]**

(a) $3.55 \times 10^{18}$ /m$^3$ (b) $3.76 \times 10^{18}$ /m$^3$
(c) $7.87 \times 10^{18}$ /m$^3$ (d) $9.94 \times 10^{18}$ /m$^3$

**3.** For intrinsic gallium arsenide , conductivity at room temperature is $10^{-6}(\Omega\text{-m})^{-1}$ , the electron and hole mobilities are, respectivities 0.85 and 0.04m$^2$V-s .The intrinsic carrier concentration at room temperature is

**[EC ESE - 2017]**

(a) $7.0\times10^{12}$m$^{-3}$ (b) $0.7\times10^{12}$m$^{-3}$
(c) $7.0\times10^{-12}$m$^{-3}$ (d) $0.7\times10^{-12}$m$^{-3}$

**4.** For which one of the following materials , is the Hall coefficient closest to zero

**[EC ESE - 2015]**

(a) Metal
(b) Insulator
(c) Intrinsic semiconductor
(d) Alloy

**5.** At temperature of 298 kelvin, silicon is not suitable for most electronic applications , due to small amount of conductivity .This can be altered by

**[EC ESE - 2015]**

(a) Gettering (b) Doping
(c) Squeezing (d) Sintering

**6.** The energy gap in the energy band structure of a material is 9eV at room temperature .The material is

**[EC ESE - 2015]**

(a) Semiconductor (b) Conductor
(c) Metal (d) Insulator

**7.** The number of holes in and N-type silicon with intrinsic value $1.5\times10^{10}$ /cm$^3$ and doping concentration of $10^{17}$/cm$^2$ , by using mass action law is

**[EC ESE - 2015]**

(a) $6.67\times10^6$/cc (b) $4.44\times10^{-25}$/cc
(c) $1.5\times10^{-24}$/cc (d) $2.25\times10^3$/cc

**8. Statement (I)** : Hall voltage is given by $V_H = R_H \frac{I.H}{t}$ where I is the current , H is the magnetic field strength , t is the thickness of probe and $R_H$ is the Hal constant
**Statement (II)** : Hall effect does not sense the carrier concentration

**[EC ESE - 2014]**

(a) Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I).
(b) Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I)
(c) Statement (I) is true but Statement (II) is false.
(d) Statement (I) is false but Statement (II) is true.

**9.** Drift velocity in a metal is

**[EC ESE - 2014]**

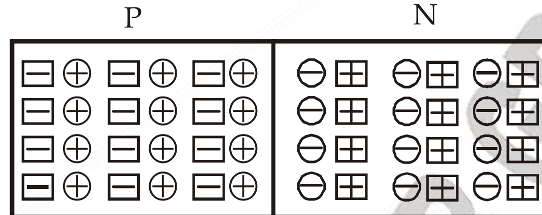
(a) Inversely proportional to the force on an electron due to applied electric field

# CHAPTER - 2

# *DIODES*

## 2.1 PN JUNCTION DIODES

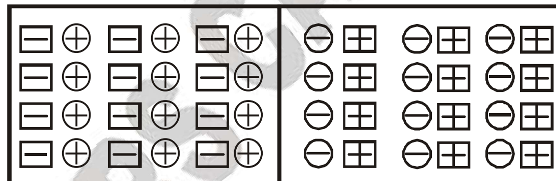
PN Junction diodes is formed by diffusing the p – type material to one side of junction and n – type of the material to other side of pn Junction i.e. the bonding force exists between p – type and n–type semiconductors.




O is Circle represents free charge carries ($e^{-s}$ and holes)

□ is Squares represents charges not free to move (Ionized donor or acceptor atoms)

### 2.1.1 Diffusion




### 2.1.2 Space Charge Region

1. Diffusion forms dipole charge layer at pn junction interface.
2. There is a ''built in'' voltage at pn junction interface that prevents penetration of $e^{-s}$ into p- side and holes into n – side.

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# ASSIGNMENT

**1.** In a uniformly doped abrupt p-n junction, the doping level of n-side is four times the doping level of p-side. The ratio of depletion layer width is:

(a) 0.25 (b) 0.5
(c) 1.0 (d) 2.0

**2.** In a junction diode:

(a) The depletion capacitance increases with increase in reverse bias.
(b) The depletion capacitance decreases with increase in reverse- bias.
(c) The diffusion capacitance increases with increase in the forward bias.
(d) The diffusion capacitance is much higher than the depletion capacitance when it is forward – biased.

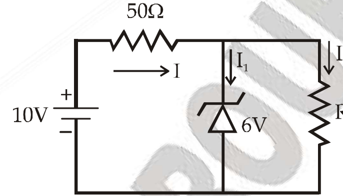
**3.** The small signal capacitance of an abrupt p-n junction is $1nF/cm^2$ at Zero bias. If the build – in voltage is 1V, the capacitance at a reverse-bias voltage of 99V is equal to:

(a)55pF (b) 75pF
(c) 100pF (d) 125pF

**4.** A p – n junction in series with a 100 Ω resistor, is forward – biased so that a current of 100 mA flows. If the voltage across this combination is instantaneously reversed to 10V at t = 0, the reverse current that flows through the diode at t = 0 is approximately given by:

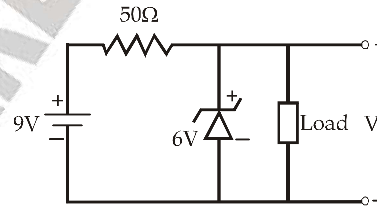
(a) Zero (b) 100 mA
(c) 200 mA (d) 50mA

**5.** The 6 V Zener Diode shown in figure has zero Zener resistance and less current of 5mA. The minimum value of R so that the voltage across it does not fall below 6V is:




(a) 70Ω (b) 80Ω
(c) 50Ω (d) Zero

**6.** A zener diode in the circuit shown in figure, has a knee current of 5mA and a maximum allowed power dissipation of 300mW. What are the minimum and maximum load currents that can be drawn safely from the circuit, keeping the output voltage $V_0$ constant at 6V?




(a) Zero, 180mA (b) 5mA, 110 mA
(c) 10mA, 55mA (d) 60mA, 180mA

**7.** Compared to a p- n junction with $N_A = N_D = 10^{14}/cm^3$, which one of the following statements is true for a p – n junction with $N_A = N_D = 10^{20}/cm^3$?

(a) Reverse breakdown voltage is lower and depletion capacitance is lower.
(b) Reverse breakdown voltage is higher and depletion capacitance is lower.
(c) Reverse breakdown voltage is lower and depletion capacitance is higher.
(d) Reverse breakdown voltage is higher and depletion capacitance is higher.

**8.** A $p^+$- n junction has a built in potential of 0.8V. The depletion layer width at a reverse –

# ASSIGNMENT

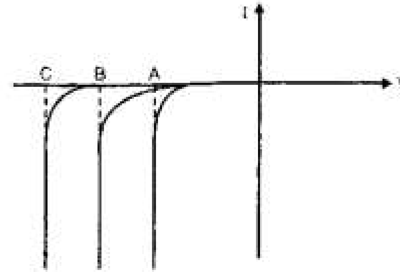
**1.** Current voltage relation for a Ge diode is given by $I = I_0 \times (e^{MV} - 1)$ at room temperature. $I_0$ is the reverse saturation current at room temperature.
Assume room temperature is 22°C. The factor M is
(a) 10 (b) 0.025
(c) 20 (d) 40

**2.** Current voltage relation for a Si diode is given by
$I = I_0 \times (e^{MV}-1)$ at room temperature, where $I_0$ is the reverse saturation current at room temperature. Assume room temperature as 72°F. The factor M is approximately
(a) 10 (b) 0.025
(c) 20 (d) 40

**Linked Statement for Q.3 & Q.4**
A voltage regulator is designed for output voltage of 25 Volts DC to a load whose maximum current is 150 mAs. Variation in input voltage is 55V to 75V.

**3.** The minimum and maximum value of series resistance shall be approximately ____ and ____ ohms. Zener diode power rating is 300 watts.
(a) 80 400 (b) 84,200
(c) 42,200 (d) 42,166.66

**4.** Shown in figure I – V characteristic of 3-diodes. $V_1$ , $V_2$, $V_3$ are the typical breakdown voltages (B.V) to be marked at points A, B, C not necessarily in the same order. Assume:
$V_1$ = B.V for ordinary pn – junction diode
$V_2$ : B.V for avalanche diode
$V_3$ : B.V for zener diode




$V_1$, $V_2$, $V_3$ should be marked at points ____, ___ and ____ respectively.
(a) A, B, C (b) C, B, A
(c) A, C, B. (d) B, C, A

**Linked Statement for Q.5 & Q.6**
Consider a Ge diode at room temperature when the voltage across it is 0.3 volt.

**5.** If the forward current for this diode is M $I_0$ where $I_0$ is the reverse saturation current at room temperature, the factor M is ….. (Assume $e^6 \approx 400$ and room temperature is 22°C)
(a) 40,000 (b) 80,000
(c) 1,60,000 (d) 3,20,000

**6.** If the temperature in case of the diode considered in (Q.5) is raised to 50°C , the ratio of the new forward current to the forward current obtained in (Q.5) shall be (Assume $e^{10} \approx$ 22,000).
(a) 1.4 (b) 2.4
(c) 3.4 (d) 4.4

**7. Assertion (A):** In the manufacture of zener diodes, silicon is usually preferred.
**Reason(R):** Silicon has higher temperature and current capability.
Choose the best alternative.
(a) Both A and R are TRUE and R is the correct explanation of A.
(b) Both A and R are TRUE and R is not the correct explanation of A.
(c) A is TRUE but R is FALSE

# GATE QUESTIONS

**1.** In a p-n junction diode at equilibrium, which one of the following statements is NOT TRUE?

**[GATE - 2018]**

(a) The hole and electron diffusion current components are in the same direction.

(b) The hole and electron drift current components are in the same direction.

(c) On an average, holes and electrons drift in opposite direction.

(d) On an average, electrons drift and diffuse in the same direction.

**2.** A p-n step junction diode with a contact potential of 0.65 V has a depletion width of 1 μm at equilibrium. The forward voltage (in volts, correct to two decimal places) at which this width reduces to 0.6 μm is _________.

**[GATE - 2018]**

**3.** Red (R), Green (G) and Blue (B) Light Emitting Diodes (LEDs) were fabricated using p-n junctions of three different inorganic semiconductors having different band-gaps. The built-in voltages of red, green and blue diodes are $V_R$, $V_G$ and $V_B$, respectively. Assume donor and acceptor doping to be the same ($N_A$ and $N_D$ respectively) in the p and n sides of all the three diodes.
Which one of the following relationships about the built-in voltages is TRUE?

**[GATE - 2018]**

(a) $V_R > V_G > V_B$ (b) $V_R < V_G < V_B$

(c) $V_R = V_G = V_B$ (d) $V_R > V_G < V_B$

**4.** A junction is made between $p^-$ S with doping density $N_{A1} = 10^{15}$ $cm^{-3}$ and p Si with doping density $N_{A2} = 10^{17}$ $cm^{-3}$.

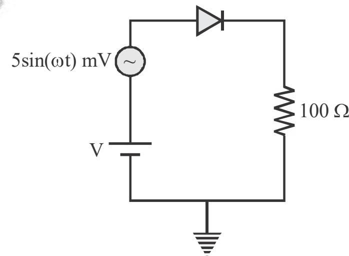
Given: Boltzmann constant $k = 1.38 \times 10^{-23}$ J. $K^{-1}$, electronic charge $q = 1.6 \times 10^{-19}$ C.

Assume 100% acceptor ionization.

At room temperature (T = 300K), the magnitude of the built-in potential (in volts, correct to two decimal places) across this junction will be ________

**[GATE - 2018]**

**5.** A DC current of 26 μA flows through the circuit shown. The diode in the circuit is forward biased and it has an ideality factor of one. At the quiescent point, the diode has a junction capacitance of 0.5 nF. Its neutral region resistances can be neglected. Assume that the room temperature thermal equivalent voltage is 26 mV.




For $\omega = 2 \times 10^6$ rad/s, the amplitude of the small-signal component of diode current (in μA, correct to one decimal place) is _______

**[GATE - 2018]**

**6.** The circuit shown in the figure is used to provide regulated voltage (5 V) across the 1 kQ resistor. Assume that the Zener diode has a constant reverse breakdown voltage for a current range, starting from a minimum required Zener current, $I_{Zmin}$ = 2 mA to its maximum allowable current. The input voltage $V_1$, may vary by 5% from its nominal value of 6 V. The

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# ESE OBJ QUESTIONS

**1.** Consider the following statements regarding the formation P-N junctions:
1. Holes diffuse across the junction from P – side to N-side.
2. The depletion layer is wiped out.
3. There is continuous flow of current across the junction.
4. A barrier potential is set up across the junction.
Which of the above statements are correct?

**[EC ESE - 2018]**

(a) 1 and 3 (b) 2 and 3
(c) 1 and 4 (d) 2 and 4

**2.** In tunnel diode, the Fermi level lies

**[EC ESE - 2018]**

(a) Inside valence band of p-type and inside conduction band of n-type semiconductors.
(b) In the energy band gap but closer to conduction band of n-type semiconductors
(c) In the energy band gap but closer to valence band of p-type semiconductor
(d) In the energy band gap but above valence band of p-type and below conduction band of n-type semiconductors

**3. Statement (I):**
The width of depletion layer of a P-N junction is increased under reverse bias.
**Statement (II):**
Junction breakdown occurs under reverse bias.

**[EC ESE - 2018]**

**Codes:**
(a) Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I)
(b) Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I)
(c) Statement (I) is true but Statement (II) is false
(d) Statement (I) is false but Statement (II) is true

**4.** Which of the following materials is used in light emitting diodes ?

**[EC ESE - 2017]**

(a) Gallium arsenide sulphate
(b) Gallium arsenide phosphide
(c) Gallium chromate phosphide
(d) Gallium phophide sulphate

**5.** In a photoconductive cell the resistance , of the semi conductor material varies with intensity of incident light.

**[EC ESE - 2017]**

(a) Directly
(b) Inversely
(c) Exponentially
(d) Logarithmically

**6.** Consider the following statements :
The main contribution to photo conduction is by
1. The generation of electron and hole pair by a photon
2.a donor electron jumping into the conduction band because of a photon’s energy
3.a valence electron jumping into an acceptor state because of a photon’s energy
Which of the above statements is/are correct ?

**[EC ESE - 2017]**

(a) 1 only (b) 2 only
(c) 3 only (d) 1, 2 and 3

**7.** A low resistance LDR of 20Ω , operated at a certain intensity of light , is to be protected through a series resistance in such a way that up to 12mA of current is to flow at a supply voltage of 10V .What is the nearest value of the protective resistance ?

**[EC ESE - 2017]**

(a) 873 Ω (b) 813 Ω
(c) 273 Ω (d) 81 Ω

**8.** Photoconductivity is a characteristic of semiconductors. When light falls on certain semiconductors , it

**[EC ESE - 2017]**

# CHAPTER - 3
# *BIPOLAR TRANSISTOR*

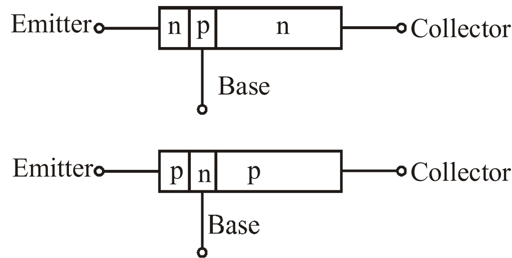
## 3.1 BIPOLAR TRANSISTOR

A transistor is basically a Si on Ge crystal containing three separate regions. It can be either NPN or PNP type the middle region is called the base and the outer two regions are called emitter and the collector. The outer layers although they are of same type but their functions cannot be changed. They have different physical and electrical properties.

In most transistors, emitter is heavily doped. Its job is to emit or inject electrons into the base. These bases are lightly doped and very thin, it passes most of the emitter-injected electrons on to the collector. The doping level of collector is intermediate between the heavy doping of emitter and the light doping of the base.

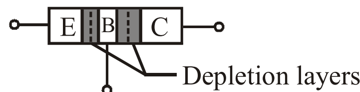
The collector is so named because it collects electrons from base. The collector is the largest of the three regions; it must dissipate more heat than the emitter or base. The transistor has two junctions. One between emitter and the base and other between the base and the collector. Because of this the transistor is similar to two diodes, one emitter base diode and other collector base diode.

When transistor is made, the diffusion of free electrons across the junction produces two depletion layers. For each of these depletion layers, the barrier potential is 0.7 V for Si transistor and 0.3 V for Ge transistor.




The depletion layers do not have the same width, because different regions have different doping levels. The more heavily doped a region is, the greater the concentration of ions near the junction. This means the depletion layer penetrates more deeply into the base and slightly into emitter. Similarly, it penetration more into collector. The thickness of collector depletion layer is large while the base depletion layer is small as shown in fig.

If both the junctions are forward biased using two D.C sources, as shown in free electrons (majority carriers) enter the emitter and collector of the transistor, joins at the base and come out of the base. Because both the diodes are forward biased, the emitter and collector currents are large.




If both the junction are reverse biased as shown in then small currents flows through both junctions only due to thermally produced minority carriers and surface leakage. Thermally produced carriers are temperature dependent it approximately doubles for every 10 degree Celsius rise in ambient temperature. The surface leakage current increases with voltage.

# WORKBOOK

**Example 1.** In a common emitter tr. at $V_{C\in} = 1V$, $V_{BE}$ is adjusted to give a collector current of 1mA keeping $V_{B\in}$ constant $V_{C\in}$ is increased to 11V find new value of $i_c$ if $V_A = 100V$.

**Solution.**

$V_{CE} = 1V$ $\quad$ $I_C = \beta I_B + I_{CE0}$

$I_C = 10^{-3}$ $\quad$ $I_C = \beta I_B + I_{CE} + I_{CE0}$

$$i_C = I_S e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{CE}}{V_A}\right)$$

$$\frac{i_C'}{i_C} = \frac{I_s}{I_s}\frac{e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{CE}}{V_A}\right)}{e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{CE}}{V_A}\right)} = \frac{1+\frac{1}{\sqrt{A}}}{\left(1+\frac{11}{100}\right)}\times 10^{-3}$$

$$i_C' = 1.11\times 10^{-3} = 1.1\text{mA}$$

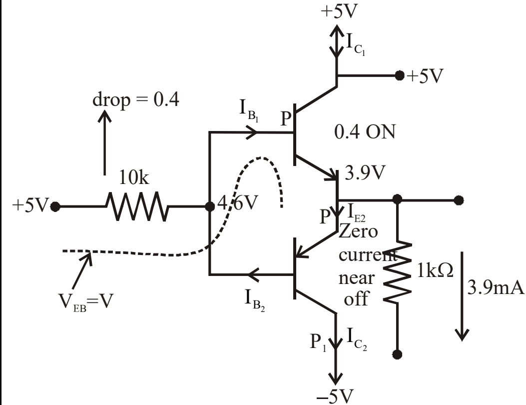
$$\text{Slope} = \frac{1\text{mA}}{1+100} = \frac{1}{101}\text{m}$$

$$\frac{IC_2 - IC_1}{11-1} = \frac{1}{101}$$

$$IC_2 = \frac{10+101}{101} = 1.1\text{wA}$$

**Example 2.** Determine all mode voltage & current through all the branches for given circuit assume $\beta = 100$.

**Solution.**




One is npn other is pnp so can′t operated simultaneously one will ON & other OFF

$I_C = 3.9$ mA

$I_E$ 3.9 39mA

$5 - I_B(10k) - 0.7 - (1k)I_E = 0$

$5 - 10I_B - 0.7 - 101\ I_B = 0$

# ASSIGNMENT

**1.** Large collector – base reverse bias is responsible for
(a) Saturation region in BJTs
(b) Reverse active mode in BJT
(c) Early effect in BJTs
(d) None of these

**Linked Statement for Q.2 & Q.3**
A transistor with $\alpha = 0.98$ and $I_{CBO} = 5\mu A$ is biased so that $I_{BQ} = I_B$ at quiescent pint = $100\mu A$

**2.** $I_{CEO}$ is
(a) $50\mu A$ (b) $100\mu A$
(c) $250\ \mu A$ (d) $500\ \mu A$

**3.** $I_{CQ}$ and $I_{EQ}$ is
(a) 5.15 mA, 5.25 mA
(b) 3mA, 315 mA
(c) 4.91 ma, 5.01 mA
(d) 27mA, 27.38 mA

**Common Data for Q. 4 to Q.5**
A Si n-p-n bipolar transistor has the following parameters:
Collector current : $I_C = 5$ mA
Common – emitter current gain factor: $h_{fe} = 100$
Operational temperature : $T = 300^oK$
Cross sectional area : $A = 10^{-8}\ cm^2$
Electron mobility : $1600\ cm^2/Vs$

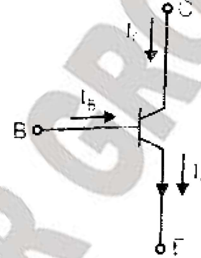
**4.** The mutual conductance is
(a) 0.19 mho (b) 0 mho
(c) $\infty$ mho (d) 3.8 mho

**5.** The input conductance is
(a) $1.9 \times 10^3$ (b) $1.9 \times 10^{-3}$
(c) $0.19 \times 10^3$ (d) $0.19 \times 10^{-3}$

**6.** The electron diffusion coefficient is (in mho)
(a) $208\ cm^2/s$ (b) $20.85\ cm^2/s$
(c) $416\ cm^2/s$ (d) $41.6\ cm^2/s$

**7.** The diffusion capacitance is
(a) 2.28 nF (b) 22.8 nF
(c) 22.85 pF (d) 2.28 pF

**8.** In the npn




$10^8$ holes /μs move from base to emitter region while $10^{10}$ electron/μs move from emitter to base region. The emitter current $I_E$ is
(a) – 1.584 mA (b) +1.84 mA
(c) + 1.616 mA (d) – 1.616 mA

**9.** Consider the following statements in respect of DIAC Vs BJT
S1: DIAC is a two terminal device whereas, BJT is a three terminal device.
S2: In DIAC, doping of each region is almost equal whereas in BJT, the doping depends upon the type of the region.
Choose the best alternative.
(a) S1 is TRUE, S2 is FALSE
(b) S1 is FALSE, S2 is TRUE
(c) Both S1, S2 are TRUE
(d) Both S1, S2 are FALSE

**10.** In order of input impedances choose the correct order for the following devices.
P. BJT in CE mode
Q. BJT in CB mode
R. MOSFET
S. JFET
(a) P < Q < S < R (b) Q < P < R < S
(c) Q < P < S < R (d) Q < S < P < R

**11.** Consider the following assertions:

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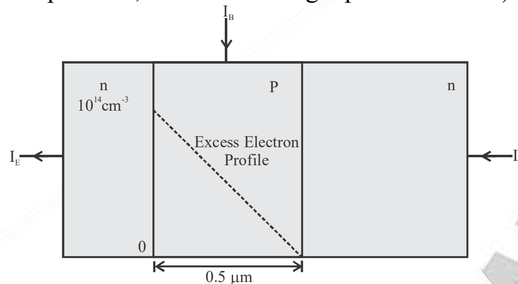
# GATE QUESTIONS

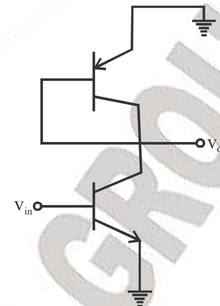
**1.** The injected excess electron concentration profile in the base region of an npn BJT, biased in the active region, is linear, as shown in the figure. If the area of the emitter-base junction is 0.001 $cm^2$, $\mu_n$ = 800$cm^2$/(V-s) in the base region and depletion layer widths are negligible, then the collector current $I_c$(in mA) at room temperature is_____ .
(Given: thermal voltage $V_T$ = 26mV at room temperature, electronic charge q = $1.6\times10^{-19}$ C)




**[GATE - 2016]**

**2.** The Ebers – Moll model of a BJT is valid
**[GATE - 2016]**
(a) Only in active mode
(b) Only in active and saturation modes
(c) Only in active and cut-off modes
(d) In active, saturation and cut-off modes

**3.** In the ac equivalent circuit shown, the two BJTs are biased in active region and have identical parameters with β>>1. The open circuit small signal voltage gain is approximately ____.
**[GATE - 2015]**




**4.** If the base width in a bipolar junction transistor is doubled, which one of the following statements will be TRUE?
**[GATE - 2015]**
(a) Current gain will increase.
(b) Unity gain frequency will increase.
(c) Emitter-base junction capacitance will increase
(d) Early voltage will increase

**5.** An n-p-n BJT having reverse saturation current $I_S$ = $10^{-15}$ A is biased in the forward active region with $V_{BE}$ = 700 mV. The thermal voltage ($V_T$) is 25mV and the current gain (β) may vary from 50 to 150 due to manufacturing variations. The maximum emitter current (in μA) is ______.
**[GATE - 2015]**

**6.** A good current buffer has
**[GATE - 2014]**
(a) Low input impedance and low output impedance
(b) Low input impedance and high output impedance
(c) High input impedance and low output impedance
(d) High impedance and high output impedance

**7.** An increase in the recombination of a BJT will increase
**[GATE - 2014]**
(a) The common emitter dc current gain

# ESE OBJ QUESTIONS

**1.** The $h_{FE}$ values in the specification sheet of a transistor are $h_{FE(max)}$ = 225 and $h_{FE(min)}$ = 64. What value of $h_{FE}$ is to be adopted in practice?

**[EC ESE - 2018]**

(a) 64 (b) 100
(c) 120 (d) 225

**2.** In a transistor, the base current and collector current are , respectively , 60μA and 1.75mA. The value if α is nearly

**[EC ESE - 2017]**

(a) 0.91 (b) 0.97
(c) 1.3 (d) 1.7

**3.** Consider the following statements regarding an N-P-N Bipolar Junction transistor :
1.Emitter diode is forward biased and collector diode is reverse biased
2.Emitter has many free electrons
3.Free electrons are injected into base and pass through collector
4.Depletion layers around junction J1 and J2 of BJT are widened
Which of the above statements are correct ?

**[EC ESE - 2015]**

(a) 1, 2 and 4 (b) 1, 3 and 4
(c) 2, 3 and 4 (d) 1, 2 and 3

**4.** Consider the following statements regarding opt couplers :
1. Opt couplers are LEDs driving photodiodes in a single package to provide electrical isolation between input and output.
2.Optocouper is LED driving a phototransistor in a single package that replaces pulse transformers working at input zero crossing
3.Optocouplers are used as temporary non fixed joints between optical fiber terminations
Which of the above statements are correct ?

**[EC ESE - 2015]**

(a) 1, 2 and 3 (b) 1 and 2 only
(c) 1 and 3 only (d) 2 and 3 only

**5.** The best device for improving the switching speeds of bipolar transistors is

**[EC ESE - 2014]**

(a) Speed –up capacitor
(b) Transistor with higher cut –off frequency
(c) Clamping diode
(d) Clamping diode with zero storage time

**6.** The early effect in bipolar junction transistor is caused by

**[EC ESE - 2014]**

(a) Fast turn off
(b) Fast turn on
(c) Large emitter to base forward bias
(d) Large collector to base reverse bias

**7.** To get higher cut –off frequency in a BJT , sheet resistance should be

**[EC ESE - 2014]**

(a) Low
(b) High
(c) Equal to cut –off frequency
(d) Zero

**8.** When a transistor is saturated

**[EC ESE - 2013]**

(a) The emitter potential is more than the base –collector potential
(b) The collector potential is more than the base –emitter potential
(c) The base potential is more than the emitter –collector potential
(d) The base , emitter and collector are almost the same potential

**9.** If the α value of a transistor changes 0.5% from its nominal value of 0.9, the percentage change is β will be

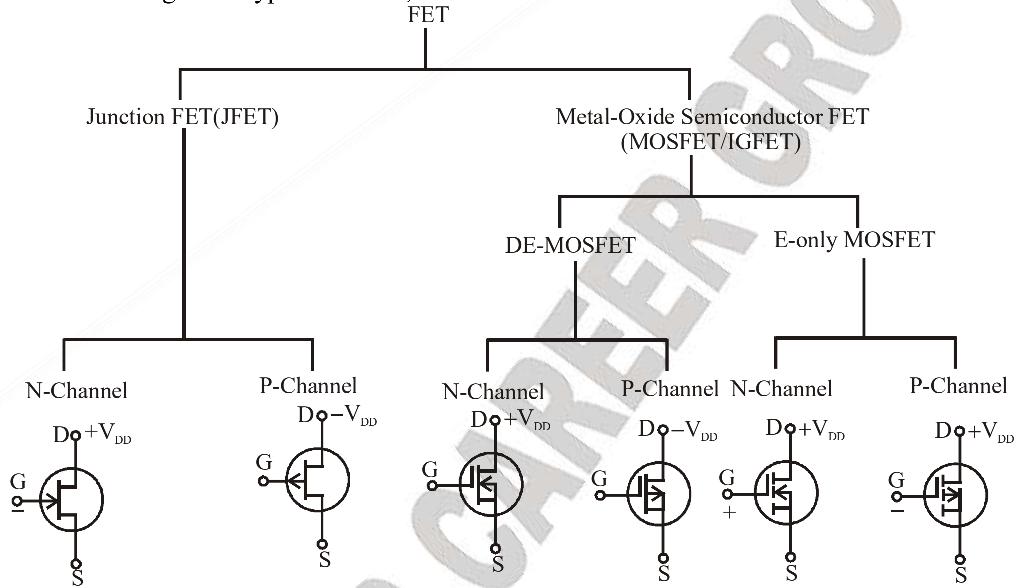
**[EC ESE - 2013]**

(a) 0% (b) 2.5%
(c) 5% (d) 7.5%

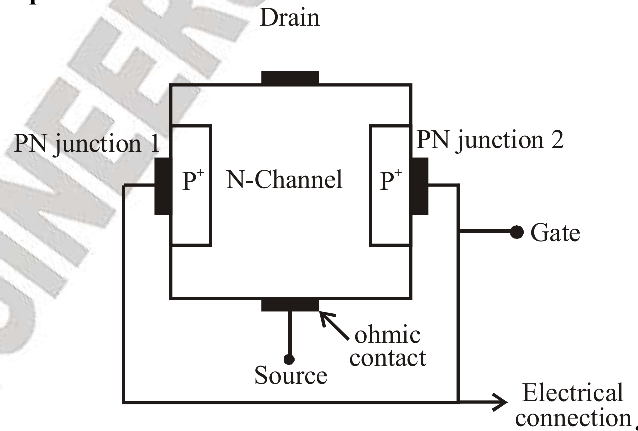
**10.** In a bipolar junction transistor an increase in magnitude of collector voltage increase the

# CHAPTER - 4
# *FIELD – EFFECT TRANSISTOR (FET)*

## 4.1 FET
### 4.1.1 Introduction
1. The Field – Effect Transistor (FET) is type of transistor that works by modulating a microscopic electric field inside a semiconductor material.
2. There are two general types of FET's, the MOSFET and JFET.




## 4.2 JFET(Junction Field Effect Transistor )
### 4.2.1 Symbol and Representation



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# WORKBOOK

**Example 1.** Consider a process technology for which $L_{min}$ = 0.4μm, $t_{ox}$ = 8nm, $\mu_n$ = 450 $cm^2$ /V.S, and $V_t$ = 0.7V. (a) Find $C_{ox}$ and $k_n'$. (b) For a MOSFET with W/L = 10, calculate the values of $V_{OV}$, $V_{GS}$, and $V_{DSmin}$ needed to operate the FET in the saturation region with a dc current $I_D$ = 100μA. (c) For the device in (b), find the values of $V_{OV}$ and $V_{GS}$ required to cause the device to operate as a 1000 Ω resistor for very small $V_{DS}$.

**Solution.**

(a) $C_{OX} = \frac{\varepsilon_{OX}}{t_{ox}} = \frac{3.45\times10^{-11}}{8\times10^{-9}}$

$= 4.32\times10^{-3}\,F/m^2 = 4.32 fF/\mu m^2$

$k_n' = \mu_n C_{ox} = 450\left(\frac{cm^2}{V}.s\right)\times 4.32 fF/\mu m^2$

= $194 \times 10^{-6}$ F/V.s = 194 μA/$V^2$

(b) For operation in the saturation region,

$i_D = \frac{1}{2}k_n'(v_{GS} - V_t)^2$

Thus, $100 = \frac{1}{2}\times 194\times\frac{8}{0.8}(V_{GS} - 0.7)^2$

Which results in $V_{GS} - 0.7 = 0.32$ V

Or $V_{GS}$ = 1.02 V

And $V_{DSmin} = V_{GS} - 0.7 = 0.32$V

For the MOSFET in the triode region with $\nu_{DS}$ very small,

$i_D = k_n'\frac{W}{L}(V_{GS} - V_t)V_{DS}$

From which the drain to source resistance $r_{DS}$ can be found as

$r_{DS} = \frac{v_{DS}}{i_D}|\text{small}\,\nu_{DS} = \frac{1}{\left[k_n'\frac{W}{L}(\nu_{GS} - V_t)\right]}$

Thus $1000 = \frac{1}{[194\times10^{-6}\times 10(\nu_{GS} - 0.7)]}$

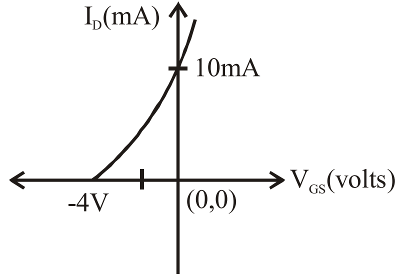
Which yields, $V_{GS} - 0.7 = 0.52V$

Or $V_{GS}$ = 1.22V

# ASSIGNMENT

**Linked Statement for Q.1 & Q.2**

Shown below is the transfer characteristics for n – channel MOSFET.




**1.** At $V_{GS}$ (Gate – to source voltage) = –2V, the $I_D$ shall be

(a) 5 mA (b) 2 mA
(c) – 2.5 mA (d) 2.5 mA

**2.** When $I_D$ is 5mA, the $V_{GS}$ will be ____ and MOSFET is _____

(a) 1.2V, enhancement type
(b) –1.2 V, depletion type
(c) 2V, enhancement type
(d) –2V depletion type

**Linked Statement for Q.3 & Q.4**

A silicon JFET at 300°K has the following parameters:

Electron density : $N_d = 1 \times 10^{17}$ cm$^{-3}$
Hole density : $N_a = 1 \times 10^{19}$ cm$^{-3}$
Relative dielectric constant = $\in_r = 11.8$
Channel height : a = 0.20 μm
Intrinsic carrier density : $n_i = 1.5 \times 10^{10}$ cm$^{-3}$

**3.** The pinch – off voltage is ≈

(a) 1.5V (b) – 1.5 V
(c) 3V (d) 6V

**4.** The built in voltage is

(a) 0.47 V (b) 3V
(c) – 3V (d) 0.94 V

**Linked Statement for Q.5 & Q.6**

A certain p-channel Si- MOSFET has the following parameters,

Doping concentration $N_a = 1.5 \times 10^{17}$ cm$^{-3}$
Relative dielectric constant ∈ = 11.8
Relative dielectric constant of $SiO_2$ : $\in_{ir} = 4$
Insulator depth : d = 0.02 μm
Operating temperature : T = 300°K
Intrinsic carrier density : $n_i = 1.5 \times 10^{10}$ cm$^{-3}$

**5.** The surface potential for strong inversion is

(a) 4V (b) 0.838 V
(c) – 4V (d) –0.838 V

**6.** The insulator capacitance is

(a) 1.77 mF/m$^2$ (b) 3.54 mF/m$^2$
(c) 5.31 mF/m$^2$ (d) 7.08 mF/m$^2$

**Linked Statement for Q.7 & Q.8**

A certain n – channel MOSFET ha the following parameters:

Channel length : L = 4 μm
Channel depth : Z = 12μm
Insulator thickness : d = 0.04 μm
Gate voltage : $V_g$ = 5V
Doping factor : m = 1
Threshold voltage : $V_{th}$ = 0.10 V
Electron mobility : $\mu_n$=1350 cm$^2$/V-s
Electron velocity : μn=1350 cm$^2$/V-s
Electron velocity : $V_s = 1.7 \times 10^7$ cm/s
Relative dielectric :
Constant of $SiO_2$ : $\in_{ir} = 4$

**7.** The insulator capacitance is ____ F/m$^2$ and saturation drain current is ____ mA

(a) $8.85 \times 10^{-4}$ , 8.85 (b) $8.85 \times 10^{-12}$, 8.85
(c) $8.85 \times 10^{-14}$ , 6 (d) $8.85 \times 10^{-9}$ , 17

**8.** The maximum operating frequency in the saturation region is

(a) 6.76 Hz (b) 6.76 MHz
(c) 6.76 GHz (d) 6.76 THz

**9.** Consider the following statements with respect to V-MOS

# GATE QUESTIONS

**1.** There are two photolithography systems: one with light source of wavelength $\lambda_1$ = 156 nm (System 1) and another with light source of wavelength $\lambda_2$ = 325 nm (System 2). Both photolithography systems are otherwise identical. If the minimum feature sizes that can be realized using System 1 and System 2 are $L_{min1}$ and $L_{min2}$ respectively, the ratio $L_{min1}/L_{min2}$ (correct to two decimal places) is_____.

**[GATE - 2018]**

**2.** Consider an n-channel metal oxide semiconductor field effect transistor (MOSFET) with a gate-to source voltage of 1.8V. Assume that $\frac{W}{L} = 4$ , $\mu_n C_{ox} = 70\times10^{-6} AV^{-2}$, the threshold voltage is 0.3V, and the channel length modulation parameter is 0.09 $V^{-1}$, In the saturation region, the drain conductance (in micro Siemens)is_______.

**[GATE - 2016]**

**3.** Consider the following statements for a metal oxide semiconductor field after effect transistor (MOSFET):
P : As channel length reduces, OFF-state current increases
Q : As channel length reduces, output resistance increases
R : As channel length reduces, threshold voltage remains constant
S: As channel reduces, ON current increases.
Which of the above statements are INCORRECT?

**[GATE - 2016]**

(a) P and Q (b) P and S
(c) Q and R (d) R and S

**4.** A voltage $V_G$ is applied across a MOS capacitor with metal gate and p-type silicon substrate at T = 300 K. The inversion carrier density (in number of carriers per unit area) for $V_G$ = 0.8 V is $2 \times 10^{11}$ $cm^{-2}$. For $V_G$ = 1.3 V, the inversion carrier density is $4 \times 10^{11}$ $cm^{-2}$. What is the value of the inversion carrier density for $V_G$ = 1.8 V?

**[GATE - 216]**

(a) $4.5 \times 10^{11}$ $cm^{-2}$ (b) $6.0 \times 10^{11}$ $cm^{-2}$
(c) $7.2 \times 10^{11}$ $cm^{-2}$ (d) $8.4 \times 10^{11}$ $cm^{-2}$

**5.** Consider a long-channel NMOS transistor with source and body connected together. Assume that the electron mobility is independent of $V_{gs}$ and $V_{DS}$. Given,
$g_m = 0.5\mu A/V$ for $V_{DS}$= 50 m V and $V_{gs}$ = 2V,
$g_d = 8\mu A/V$ for $V_{gs}$ = 2 V and $V_{DS}$ = 0 V,
Where $g_m = \frac{dI_D}{dV_{gs}}$ and $g_d = \frac{dI_D}{dV_{DS}}$
The threshold voltage (in volts) of the transistor is

**[GATE - 2016]**

**6.** A long-channel NMOS transistor is biased in the linear region VDS = 50 mV and is used as a resistance. Which one of the following statements is NOT correct?

**[GATE - 2016]**

(a) If the device width W is increased, the resistance decreases
(b) If the threshold voltage is reduced, the resistance decrease
(c) If the device length L is increased, the resistance increases
(d) If VGS is increased, the resistance increases

**7.** In a MOS capacitor with an oxide layer thickness of 10 mm, the maximum depletion layer thickness is 100 mm. The permittivity's of the semiconductor and the oxide layer are $\varepsilon_\delta + \varepsilon_{ox}$ respectively. Assuming $\frac{\varepsilon_s}{\varepsilon_{ox}}$ the ratio of the maximum capacitance to the minimum capacitance of this MOS capacitor is ___________.

**[GATE - 2015]**

# ESE OBJ QUESTIONS

**1.** For an n-channel silicon JEET with a = 2 × $10^{-4}$ cm and channel resistivity ρ – 5Ω-cm, $\mu_n$ = 1300 $cm^2/V$–s and $\varepsilon_0 = 9 \times 10^{-12}$ F/m, the pinch off voltage, $V_p$, is nearly

**[EC ESE - 2018]**

(a) 2.30 V (b) 2.85 V
(c) 3.25 V (d) 3.90 V

**2.** For JFET , the drain current $I_D$ is :

**[EC ESE - 2017]**

(a) $I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^{1/2}$ (b) $I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)$

(c) $I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^{3/2}$ (d) $I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^{2}$

**3.** Thermal runaway is not possible in FET because as the temperature of the FET increase

**[EC ESE - 2017]**

(a) Mobility decreases
(b) Trans – conductance increases
(c) Drain current increases
(d) Trans – conductance decreases

**4. Statement (I) :** The gate of MOSEFT is insulated from the body of FET by deposition of a very thin fragile layer of $SiO_2$ over the substrate

**Statement (II) :** The device is therefore called as an insulator gate field –effect transistor (IGFET)?

**[EC ESE - 2012]**

(a) Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I).
(b) Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I)
(c) Statement (I) is true but Statement (II) is false.
(d) Statement (I) is false but Statement (II) is true.

**5.** A gate of drain –connected enchancement mode MOSFET is an example of

**[EC ESE - 2012]**

(a) An active load
(b) A switching device
(c) A three –terminal device
(d) A diode

**6.** Thermal run-away is not possible in FET because , as the temperature of FET increases ?

**[EC ESE - 2012]**

(a) The drain current increases
(b) The mobility increases
(c) The mobility decreases
(d) The transconductance increases

**7.** Consider the following statements related to JFET :?

1.Its operation depends on the flow of minority carriers only
2. It is less noisy than BJT
3. It has poor thermal stability
4. It is relatively immune to radiation

The correct statements are

**[EC ESE - 2012]**

(a) 1, 2, 3, 4 (b) 1 and 2 only
(c) 2 and 4 only (d) 3 and 4 only

**8.** Body effect in MOSFETs result in

**[EC ESE - 2012]**

(a) Increase in the value of Transconductance
(b) change in the value of threshold
(c) decrease in the value of Transconductance
(d) increase in the value of output resistance

**9. Assertion (A)** : The resistance of a FET in non-conducting region is very high

**Reason (R)** : The FET is semiconductor device

**[EC ESE - 2012]**

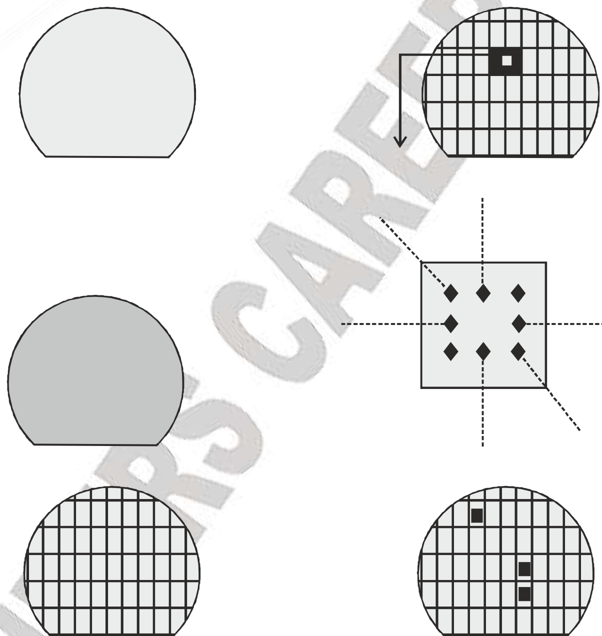
(a) Both A and R are individually true and R is the correct explanation of A

# CHAPTER - 5
# *INTEGRATED CIRCUIT FABRICATION*

## 5.1 INTRODUCTION

The starting material for integrated circuit (IC) fabrication is the single crystal silicon water. The end product of fabrication is functioning chips that are ready for packaging and final electrical testing before being shipped to the customer. The intermediated steps are referred to as water fabrication (in cluding sort). Water fabrication refers to the set of manufacturing processes used to create semiconductor devices and circuits.

Some common water terminology used are chip, die, device, circuit, and microchip. These refer to patterns covering the water surface that provide specific functionality. The terminology die and chip are most commonly used and interchangeably refer to one standalone unit on the water surface. Thus, a water can be said to be divided into many dies or chips, and shown in figure.



Schematic of water showing the division into individual dies. One individual die with electrical contacts is also shown. Some of these dies are used for testing. Dies at the edge dies are incomplete. Adapted from Microchip Fabrication – Peter Van Zant.
Schematic of various components of a water.
1.Chip
2.Scribe
3.Line
4.Test die
5.Edge chips
5.Water Crystal Plane

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# ASSIGNMENT

**1.** Consider the following sentences with regard to integrated circuits:
S1: isolation in ICs is required to avoid thermal run away for transistors.
S2: Metalization process is to interconnect the various circuit elements.
Choose the best alternative.
(a) S1 is TRUE , S2 is FALSE
(b) S1 is FALSE , S2 is FALSE
(c) Both S1, S2 are TRUE
(d) Both S1, S2 are FALSE

**2.** Consider the following statements:
S1 : Xl – rays are used for lithography in IC technology because they can be focused easily.
S2: The basic function of 0.5 buried $n^+$ layer in an n-p-n transistor in IC is to reduce the collector series resistance.
With regard to integrated circuits fabrication, choose the best alternative.
(a) S1 is TRUE, S2 is FALSE
(b) S1 is FALSE, S2 is TRUE
(c) Both S1, S2 are TRUE
(d) Both S1, S2 are FALSE

**3.** **Assertion (A):** Usually in ICs it is easy to fabricate transistor of n-p-n type.
**Reason (R):** Collector is of n-type, because n-type impurities have smaller values of diffusion constant.
Choose the best alternative.
(a) Both A and R are true and R is the correct explanation
(b) Both A and R are true and R is not the correct explanation of A
(c) A is true, but R is false
(d) A is false, but R is true

# SOLUTIONS

**Sol.1. (b)**
Isolation is required to minimize electrical interaction between circuit components.

**Sol.2. (b)**
X-rays high resolution capacity makes it usable in lithography.

**Sol.3. (a)**
Collector is subjected to heating during the base and emitter diffusion

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# ESE OBJ QUESTIONS

**1.** When the photo resist coating * during IC fabricating exposed to ultraviolet light the photo resist becomes

**[EC ESE - 2013]**

(a) Oxidised (b) Ionized
(c) Polymerised (d) Brittle

**2.** The p – type epitaxial layer grown over an n – type substrate for fabricating a bipolar transistor will function as

**[EC ESE - 2011]**

(a) The collector of a p – n –p transistor
(b) The base of an n – p – n transistor
(c) The emitter of a p – n – p transistor
(d) The collector contact for p – n – p transistor.

**3.** The maximum concentration of the element which can be dissolved in solid silicon at a given temperature is termed as

**[EC ESE - 2009]**

(a) Solid solubility
(b) Dissolution coefficient
(c) Solidification index
(d) Concentration index

**4.** The process of extension of a single – crystal surface by growing a film in such a way that the added atoms form a continuation of the single – crystal structure is called

**[EC ESE – 2009]**

(a) Ion implantation
(b) Chemical vapour deposition
(c) Electroplating
(d) Epitaxy

**5.** Why is the term 'planer technology' for fabrication of devices in ICs used?

**[EC ESE - 2008]**

(a) The variety of manufacturing processes by which devices are fabricated, takes place through a single plane
(b) The aluminium contacts to the collector, base an emitter regions of the transistors in the ICs are laid in the same plane
(c) The collector, base and emitter regions of the transistors in ICs are laid in the same plane
(d) The device looks like a thin plane water

**6.** Which of the following capacitors are made use of widely for a capacitance application in monolithic ICs.
(i) MOS capacitor
(ii) Collector Substrate capacitor
(iii) Collector base capacitor
(iv) Base – Emitter capacitor
Select the correct answer using the code given below

**[EC ESE - 2008]**

(a) i and ii only (b) ii and iii only
(c) iii and iv only (d) i and iv only

**7. Assertion (A):** The resistors and capacitors fabricated using IC technology have poor tolerances with respect to their absolute values.
**Reason (R):** As all the components of the IC are fabricated simultaneously, their ratio of tolerances is very low.

**[EC ESE - 2007]**

(a) Both (A) and (R) are individually true and (R) is the correct explanation of (A).
(b) Both (A) and (R) are individually true but (R) is not the correct explanation of (A).
(c) (A) is true but (R) is false.
(d) (A) is false but (R) is true.

**8.** In integrated circuits, the design of electronic circuits is based on the approach of use of

**[EC ESE - 2006]**

(a) maximum number of resistors in the circuit
(b) large sized capacitor
(c) minimum chip area irrespective of the type of components in the design
(d) Use of only bipolar transistor



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